

The background of the entire slide is a dark blue, high-contrast image of a microchip or circuit board. It features a dense grid of small, square components, likely logic gates or memory cells, arranged in a regular pattern. The lighting is slightly uneven, creating a sense of depth and highlighting the intricate details of the chip's surface.

SLEC[®]

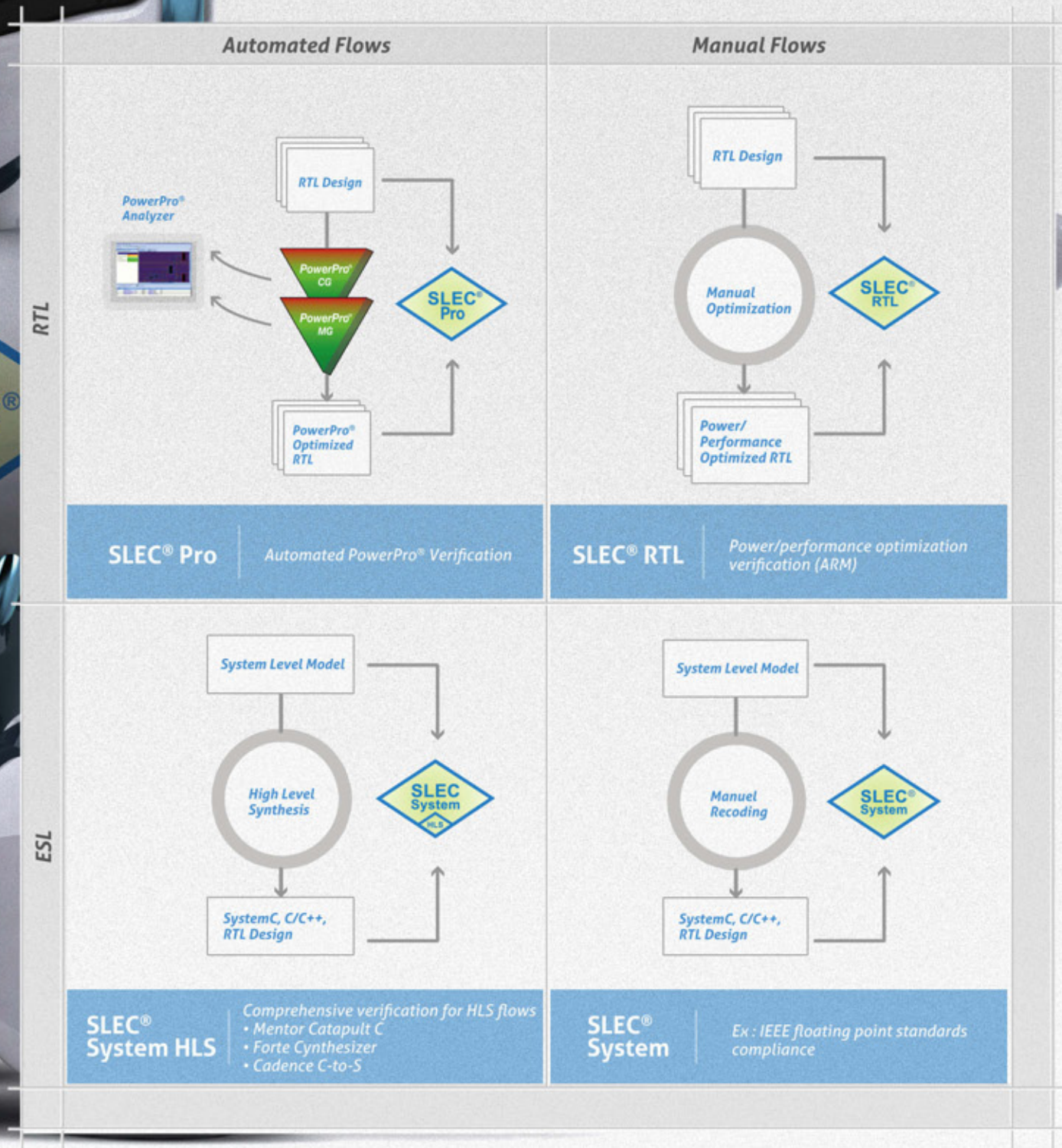
Sequential Logic Equivalence Checking
Product Family

It's functional verification, on a whole new level.



The emergence of consumer electronics is causing a fundamental shift in Register Transfer Level (RTL) design methodologies. The race for time to market has resulted in adoption and growth of higher level design creation methodologies. In particular, High Level Synthesis (HLS) directly from software models to hardware has become very popular. On the other end of the spectrum, the need to create faster and lowest power RTL designs for consumer devices has lead to design flows where designers use aggressive techniques and tools for optimizing a given RTL design for frequency and power. However, with new design techniques emerges the challenge of verification. There is a significant need for next generation equivalence checking solutions which verify software models against the HLS generated RTL as well as various optimized versions of an RTL design against the original RTL. Traditional combinational equivalence techniques are not applicable to these next generation problems. There is need in the market for sequential equivalence which can check designs with extremely different internal state.

Based on Patented Sequential Analysis Technology



SLEC is the only sequential logic equivalence checking family available in the industry today. Based on our patented Sequential Analysis Technology, SLEC verifies designs across abstractions, state, timing and interface differences. By verifying that both designs produce the same output for all possible inputs, over all time, the quality of verification that SLEC performs in minutes is equal to years of running simulation. Because SLEC does not require testbenches or assertions, engineers spend significantly less time developing their verification environment and more time creating quality design. The SLEC family consists of four products.

- // SLEC Pro provides automatic formal equivalence checking, to ensure the functionality of your design remains correct when you use the PowerPro optimization platform in your design flow.
- // SLEC RTL functionally verifies RTL designs manually optimized for power and performance. It is a very effective optimization verification solution for high performance, low power design teams (e.g. optimizing ARM cores).
- // SLEC System proves that a refined system-level model or RTL implementation is functionally equivalent to the original system-level model.
- // SLEC System-HLS extends the benefits of SLEC System to ESL design flows by comprehensively verifying the RTL generated from High Level Synthesis (HLS). It is integrated with the leading HLS tools in the market (Mentor Catapult, Cadence C-to-S, Forte Cynthesizer).

Key Differentiators

- // Unique word level solvers which are critical for equivalence checking of designs with complex control and arithmetic
- // Hardware model extraction from software languages like C/C++
- // Strong sequential proofs engine which deploys techniques like induction for complete proof for designs with complex states
- // Tight integration with HLS partner products (Mentor Catapult, Cadence CtoS, Forte Cynthesizer) for a completely automated synthesis and equivalence checking flow
- // Production proven with over 100 tapeouts across all industry segments and design types

Sampling of Blocks verified by SLEC®

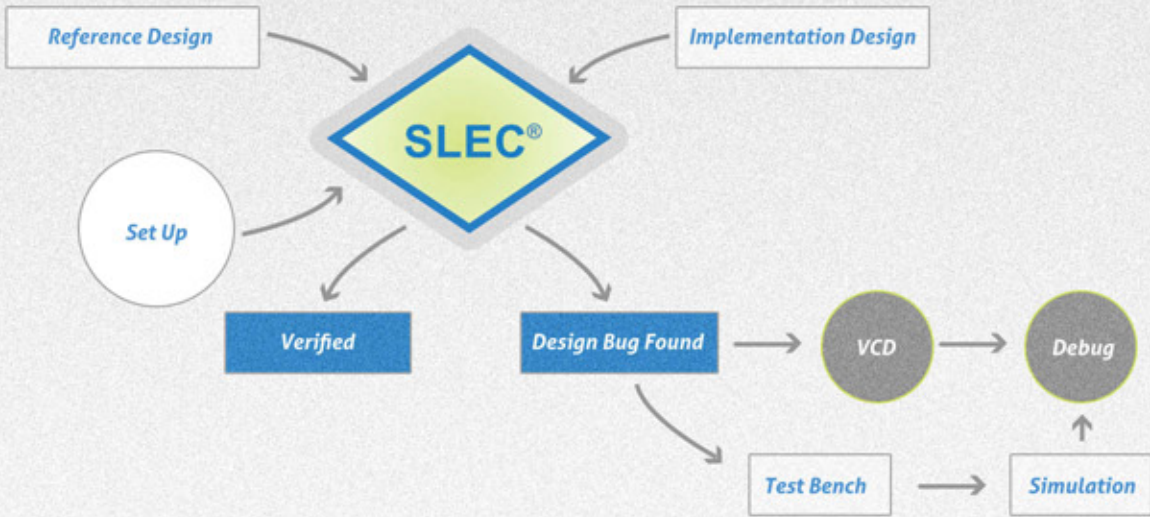
- | | |
|---|--------------------------|
| // Instruction pipeline :
ARM, MIPS, PowerPC, SH, V850 | // Ultra wideband filter |
| // DSP: C-XX | // Floating point unit |
| // MPEG4 dct/idct | // 3D graphic processor |
| // H.264 scaling algorithm | // Arithmetic logic unit |
| // Memory controller | // Memory cache |
| // H.264 interleaver | // Gaussian filter |
| // Wireless baseband DSP | // Audio Encoder/decoder |
| // Weiner filter | // Vector processor |
| // Encryption | // Audio Equalizer |
| // Video Mapper | // PCI express core |

Integrated into Existing Design Flows

SLEC integrates seamlessly into the existing visual debugging aids by generating waveforms highlighting the difference between designs being checked. These waveforms can be directly viewed in a debugger of your choice with a single command.

SLEC integrates with industry standard simulation environments and generates testbenches which can highlight the difference between the two designs when they are run in your standard simulation flow.

SLEC is controlled through a TCL interface that is organized into three basic functions: setup, map and verify. Setup commands specify the design, library and constraint files. Map commands specify input and output maps as well as state point maps if they exist (with relevant timing information). Verify command and associated settings control the optimal performance of SLEC as it proves the equivalence.



Benefits

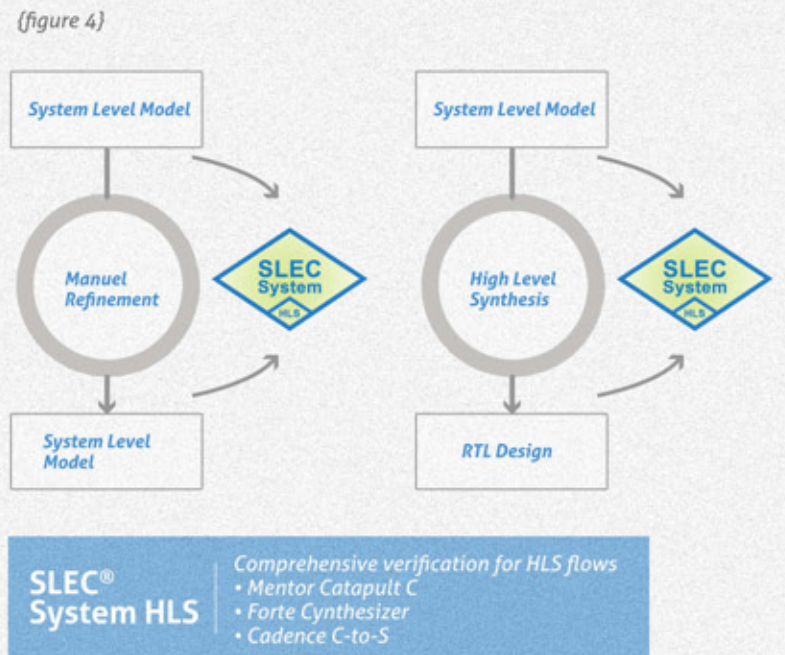
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|--|--|
| // Does not require 1-1 state point or I/O maps | // Ensures hardware intent remains unchanged during system-level model refinement |
| // Verifies without testbenches or assertions | // Integrates with industry leading high-level synthesis tools |
| // Leverages system-level models to verify RTL designs | // Replaces time consuming simulation regressions with fast results |
| // Quickly finds bugs that other tools miss | // Enables aggressive RTL power and timing optimizations by providing formal verification sign-off |
| // Isolates bugs with short, concise debug waveforms | |

SLEC® Product Details



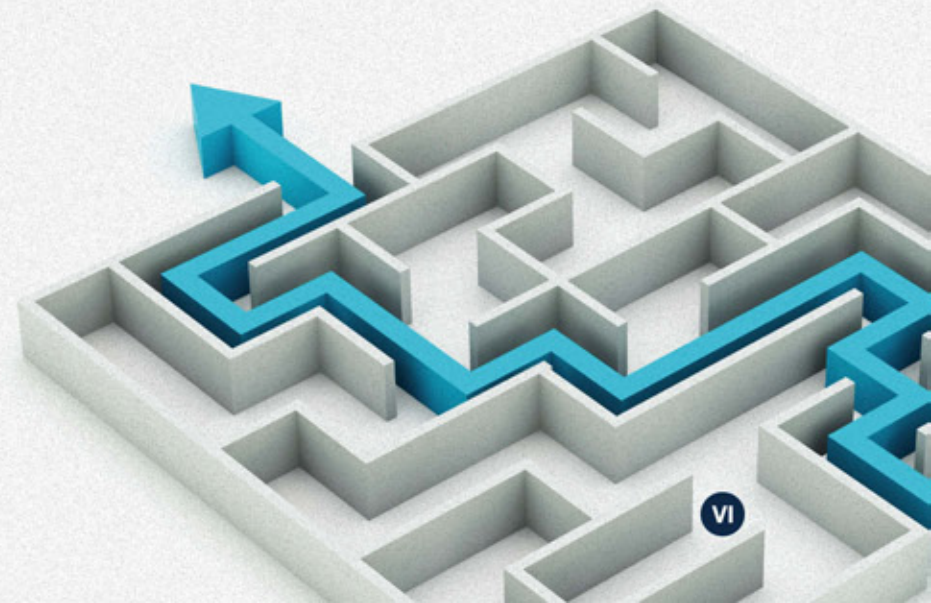
Applications: HLS Sign-off Checking for Mentor Catapult, Cadence C-to-S and Forte Synthesizer

SLEC System-HLS is a good fit for all design teams which are using High Level Synthesis as part of their RTL design flow. It is fully integrated with the above mentioned industry standard HLS tools resulting in an easy to use synthesis and verification flow. It provides a comprehensive signoff of the RTL functionality generated by HLS and is a key enabler in the adoption of HLS. C-C equivalence checking is another very useful application of SLEC System HLS. The need for this verification arises often in a HLS flow where the C/SC model is refined multiple times to get the best quality of results from HLS. SLEC System-HLS is used to ensure that no refinement iteration compromises the original functionality. Figure 4 shows the two use models of SLEC System-HLS in the design flow.



Popular Applications: IEEE Compliance Checking of Floating Point RTL's, Checking Functional Correctness of C Model Refinements or C-C Equivalence Checking

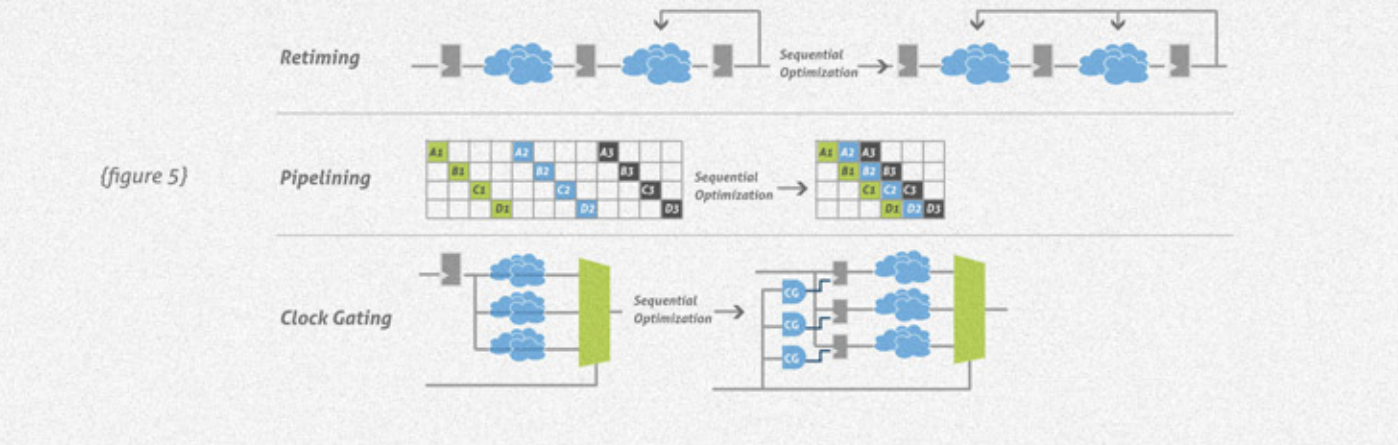
SLEC System is a good fit for design teams verifying their RTL blocks by simulating them against functional C/C++/SystemC models. The system models can be leveraged completely for verifying the RTL blocks without the need for testbenches and testplans using a simple Tcl setup. SLEC System is a popular solution for verification of IEEE compliant floating point arithmetic designs. An inbuilt IEEE compliant C++ library is used by SLEC as a reference model to equivalence check floating point RTL implementations. Calypto's unique Word Level Solver technology enables verification of floating point multipliers which was earlier not possible. The floating point RTL verification has been a significant pain point which often takes more than 6 months of simulation effort while suffering from low coverage. SLEC System Manual has reduced the effort from months to weeks. Automatic wrapper and TCL setup generation make SLEC System intuitive and easy to use.



SLEC® Product Details



Popular Application: Verification of RTL Level Power and Timing Optimizations for ARM Cores



SLEC RTL is a good fit for high performance and low power RTL design teams. With SLEC RTL designers can make aggressive optimizations which often involve micro-architectural changes to the RTL blocks. In particular merging or splitting flops, re-encoding states, re-pipelining, retiming and clock gating can be completely and exhaustively verified by SLEC RTL without the need for time consuming simulations. Figure 5 shows some of the transforms verified by SLEC RTL. Design teams working on microprocessor cores use it for verifying all functionality preserving manual RTL edits before checking them in. This lends stability to the full chip regressions and takes significant workload away from simulation farms. SLEC RTL has been used in multiple processor tapeouts and is a very popular solution for ARM core RTL optimization teams.



Application: Full Automatic Verification of Power Optimizations Performed by Calypto's PowerPro Family

SLEC Pro is a fully automatic formal verification solution for RTL blocks optimized by Calypto's PowerPro SoC low power design platform. It comes with unique technology specifically targeted for the class of power optimizations performed by PowerPro CG and PowerPro MG. It is currently used as a standard verification solution by almost all PowerPro customers.

- System Requirements and Compatibility**
- Languages: VHDL 87, 93 & 97, Verilog 95 & 2001, System Verilog
 - High Level Synthesis Integrations: Mentor Catapult, Cadence C-to-S, Forte Synthesizer
 - Simulation and Debug Environment: Novas Debussy/Verdi, Cadence NC/Simvision, Synopsys VCS, Mentor Modelsim
 - Operating Systems: Redhat Enterprise Linux 3.0 and 4.0
 - Platforms: 32-bit and 64-bit x86 compatible hardware
 - Memory: 2 GB minimum



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Empowering *the next* level of design