NEWS RELEASE

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Calypto Reduces Runtime by 6X with Release of SLEC 5.1

Groundbreaking verification and modeling techniques dramatically improve design team efficiency

SANTA CLARA, Calif. — January 10, 2011 — Calypto Design Systems Inc., the leader in sequential analysis technology, today announced the release of SLEC® 5.1 which includes breakthrough verification and modeling techniques for dramatically reduced runtimes. New deep-loop and stall verification techniques for ESL flows, and "symbolic" memory modeling, enable runtime improvements of up to 6X. SLEC is the industry's only comprehensive functional verification solution that formally verifies equivalence between ESL models and RTL implementations.

"The innovative techniques in SLEC 5.1 enable the verification of a whole new class of designs in terms of size and complexity, and dramatically increase designer productivity," said Gagan Hasteer, Sr. VP of engineering of Calypto Design Systems. "SLEC 5.1 reduces verification time from hours to minutes, enabling designers to focus their valuable time on creating a unique solution for their end application."

SLEC 5.1 includes the unique ability to verify designs in the presence of deep loops and stall conditions without the need to specify any constraints, eliminating the need for time-consuming simulation verification. The deep-loop feature is now fully integrated into SLEC's design flow for verifying HLS designs, providing a seamless solution for HLS tool users.

Support for Symbolic Modeling of Memories

SLEC 5.1 includes support for "symbolic" memory models, enabling efficient, accurate verification of arrays and memories in designs. Previously, designers were forced to model memories and arrays manually, a costly, time-consuming and error-prone process.

SLEC Family of Products

The SLEC family of products includes:

- **SLEC System**: Formally verifies equivalence of system-level models and RTL designs.
- **SLEC System-HLS**: Formally verifies that an RTL design generated using high-level synthesis is functionally equivalent to its corresponding system level model.
- **SLEC RTL:** Formally ensures functional equivalence between a golden RTL model and a corresponding RTL model has been sequentially modified to reduce power or improve performance.
- **SLEC Pro**: Comprehensively verifies that an RTL design generated by Calypto's PowerPro product is functionally equivalent to its corresponding golden RTL model.

Pricing and Availability

Available now, Calypto's SLEC 5.1 runs on PC platforms running Linux. Pricing for a one-year, time-based license is as follows:

SLEC System: $250,000

SLEC System-HLS (add on option to SLEC System): $50,000

SLEC RTL: $175,000

SLEC Pro: $125,000

About Calypto

Founded in 2002, Calypto® Design Systems, Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class RTL power optimization and functional verification software, based on its patented sequential analysis technology. Calypto, whose customers include Fortune 500 companies worldwide**,** is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor program, Si2 and is an active participant in the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America. Corporate headquarters is located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. More information can be found at: www.calypto.com.

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