NEWS RELEASE

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Calypto Broadens Industry's Most Comprehensive Power Optimization Product Family with New PowerAdviser Flow

Leverages sequential analysis technology to deliver most complete RTL power optimization solution

SANTA CLARA, Calif. — January 19, 2010 — Calypto® Design Systems Inc. (www.calypto.com), the leader in sequential analysis technology, today announced a new PowerAdviser Flow that enables designers to deliver the most power-optimized SoC designs possible. Using sequential design information generated by Calypto's popular PowerPro CG and PowerPro MG tools, the PowerAdviser Flow provides users with specific design changes that can be manually implemented in their RTL code to reduce power. The award-winning PowerPro product family is used by the world's leading SoC designers for networking, computer, consumer, and wireless applications.

"Our goal is to provide SoC designers with the most comprehensive RTL power optimization platform available, enabling the creation of devices with the lowest power consumption possible despite increasing design complexity," said Tom Sandoval, chief executive officer of Calypto Design Systems. "With our PowerAdviser Flow, designers now have the capability to easily achieve their power goals through either automated or manual RTL optimization."

PowerAdviser Flow Reduces Power Optimization Task Time from Days to Hours

Identification of RTL modifications for power savings can represent up to 50 percent of the total manual power optimization effort. The PowerAdviser Flow automates the process of thoroughly investigating power optimization opportunities in an RTL design using the visualization capability provided by Calypto's PowerPro Analyzer tool. Designers can therefore more quickly understand where to invest design time for power reduction.

The PowerAdviser Flow presents design optimizations in the form of RTL changes, schematics, and textual descriptions. Quantifiable power savings for every potential optimization is provided in the form of a hyperlinked table.

Opportunities for power optimization are provided to the user based on three methods:

- *Enable Expression Visualization* : Displays enable expressions that are automatically generated by PowerPro. The expressions can be directly inserted into the RTL by the designer.
- *Enable Expression Assistance* : Displays changes to the RTL that would result in the identification of additional clock gating/memory gating opportunities by PowerPro. Once the changes to the RTL are made, PowerPro is rerun to generate the enable expressions that can be directly inserted into the RTL.
- *MicroArchitecture Assistance*: Identifies design regions using PowerPro generated statistics (power, clock-gating efficiency, toggle data, etc.) where micro-architectural modifications would result in identification of additional clock gating/memory gating opportunities by PowerPro. Once the modifications are made, PowerPro is rerun to generate the enable expressions that can be directly inserted into the RTL.

Once the RTL changes are made, Calypto's popular SLEC® RTL product is used to comprehensively verify that the new power-optimized RTL is functionally equivalent to the original RTL.

PowerPro 3.1 Adds New Features Aimed at Power Optimization

The PowerAdviser Flow is available in the PowerPro 3.1 release. In addition to the PowerAdviser Flow, the PowerPro 3.1 release includes new features and capabilities to reduce power in logic, registers, clocks, and embedded memories, including new sequential optimization techniques to reduce dynamic and leakage memory power, ECO support, and 64-bit support for optimizing larger designs.

About PowerPro Products

The PowerPro product family is the industry's most comprehensive RTL power optimization platform and includes PowerPro CG, PowerPro MG, PowerPro Analyzer and the new PowerAdvisor Flow. Using PowerPro, designers can significantly lower power across an SoC design while reducing overall design time.

PowerPro CG is an automated RTL power optimization tool that reduces power by up to 60 percent with little or no impact to timing or area. PowerPro CG reads in an RTL design and evaluates circuit behavior across multiple clock cycles to identify sequential clock gating enable

conditions. PowerPro CG then generates new low-power RTL that looks identical to the original RTL with the addition of sequential clock gating logic.

PowerPro MG is an automated memory power optimization solution that takes advantage of the low-power control options available in today's on-chip memories to reduce both dynamic and leakage memory power with little or no impact to timing or area. PowerPro MG reduces dynamic power by automatically generating logic to control the memory enable signal to eliminate unnecessary memory accesses. PowerPro MG reduces leakage power by automatically generating logic to control the sleep modes of individual embedded memories.

PowerPro Analyzer is the industry's most accurate register-transfer level (RTL) power analysis tool. PowerPro Analyzer PowerPro Analyzer also provides complete visualization of PowerPro CG and PowerPro MG optimizations, allowing users to view power optimizations in the context of RTL source code, schematic display, sortable reports (ASCII, HTML, CSV, XML), and design hierarchy. PowerPro Analyzer is used in the PowerAdviser Flow to provide the design and power information that designers can use to manually power optimize their design.

Pricing and Availability

Available now, Calypto's PowerPro 3.1 runs on PC platforms running Linux. PowerPro CG and PowerPro MG are each priced at $295K for a one-year, time-based license. PowerPro Analyzer is included with either PowerPro CG or PowerPro MG. Current PowerPro customers will be upgraded to the version 3.1, which includes the PowerAdviser Flow.

About Calypto

Founded in 2002, Calypto® Design Systems, Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class power optimization and functional verification software, based on its patented sequential analysis technology. Calypto, whose customers include Fortune 500 companies worldwide**,** is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor program, Si2 and is an active participant in the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America. Corporate headquarters is located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. More information can be found at: www.calypto.com.

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