NEWS RELEASE

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ARC, Calypto Team to Reduce Power in ARC's Video Subsystem Solution

Calypto's PowerPro CG Reduces Power by 15 Percent on Previously Optimized Design

SANTA CLARA, Calif. — January 21, 2009 — Calypto™ Design Systems Inc., the leader in sequential analysis technology, today announced its collaboration with ARC International (LSE: ARK) to reduce power in ARC's low-power video subsystem intellectual property (IP) solution using Calypto's PowerPro CG. ARC's popular video subsystems are ideal for applications such as high-end cell phones, digital video recorders, webcams, and portable media players to provide encoding and/or decoding functionality. The announcement today showcases the ability for designers to further reduce power in their IP blocks, such as ARC's, for System on a Chip (SoC) design in a variety of applications.

"Enabling our customers to build unique, low-power solutions with our multimedia subsystems is a first-order priority," remarks Paul Holt, ARC's vice president, SoC business unit. "PowerPro CG's ability to further reduce power in our IP offering will be beneficial to our customers, many of whom are tasked with meeting ever-shrinking power budgets in portable devices."

ARC licenses award-winning consumer intellectual property (IP) in the form of multimedia subsystems and related technologies to semiconductor and OEM companies worldwide.

Calypto's PowerPro CG is the industry's only automated register transfer level (RTL) power optimization tool. PowerPro CG inserts advanced sequential clock gating structures into an RTL design and is proven to reduce power by up to 60 percent on customer designs.

"PowerPro CG has once again demonstrated its ability to reduce power in a fully automated flow, even on designs that are already highly optimized for low-power applications," said Tom Sandoval, CEO of Calypto Design Systems. "Design teams, worldwide, are benefiting from this 'must-have' tool for low-power flows."

Further Reducing Power in ARC's AV401 Video Subsystem—by up to 15 Percent

PowerPro CG was able to significantly reduce power on ARC's AV401 video subsystem in a high-performance H.264 application, translating into a measured power savings of 15 percent in this particular design operating at 200 MHz. The ARC AV401 is a user-configurable video decoding platform that provides video decoding for multiple standards to allow playback of virtually any content. While the AV401 is already a low-power video decode platform, PowerPro CG was applied to the design of the video codec, showcasing how PowerPro CG can be applied by a user to ARC's configurable IP block to further reduce power for a variety of video applications.

PowerPro CG reads in a synthesizable RTL design and generates a new RTL design which is an identical to the original design with additional clock-gating enable

logic. The low-power RTL is then comprehensively verified using sequential logic equivalence checking to ensure no functional changes are introduced.

About Calypto

Founded in 2002, Calypto Design Systems, Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class power optimization and functional verification software, based on its patented sequential analysis technology. Calypto, whose customers include Fortune 500 companies worldwide**,** is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor program, Si2 and is an active participant in the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America. Corporate headquarters is located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. More information can be found at: www.calypto.com.

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