Calypto Launches Industry's Most Advanced RTL Power Optimization Platform

PowerPro 5.0 deploys unique sequential optimization techniques and RTL power analysis for SoC power reduction; Improves runtime by 2X

SANTA CLARA, CA – May 26, 2011 -- Calypto® Design Systems, Inc., the leader in sequential analysis technology, today announced version 5.0 of its **PowerPro**® Platform, a full suite of RTL power optimization tools proven to reduce power by up to 60 percent on multi-million gate designs. The PowerPro Platform features new RTL power analysis capabilities, production-proven optimization techniques for reducing dynamic and leakage power in the logic, memory, and embedded processor sections of an SoC, and is the only solution that provides sequential formal equivalence checking.

Version 5.0 of the PowerPro Platform improves turnaround time by 2X and includes new usability features such as advanced reset-logic insertion, bottom-up flow support, a stronger sequential analysis engine for PowerPro MG (Memory Gating), and the ability to read the Fast Signal Database (FSDB), which eliminates the need for large Value Change Dump (VCD) files. In addition, each PowerPro module can run in a fully automatic or a manual mode, giving users the flexibility to select the use mode most appropriate for each section of their design. The manual use mode graphically illustrates the power reducing RTL modifications that can be made, but leaves it up to the user to decide how best to implement them.

"Our PowerPro Platform is the clear industry leader in RTL Power Optimization," noted Anmol Mathur, CTO, Calypto Design Systems. "PowerPro delivers superior QoR, and consistently matches or exceeds what a designer can do manually. In addition to a manual use model, the usability and run time improvements in PowerPro 5.0 are allowing PowerPro to be used in a fully automatic flow by several customers. This reduces project cycle time and is ideal for applications where the team does not have a deep understanding of the block, such as in IP reuse."

About the PowerPro Platform

PowerPro is the industry's most comprehensive RTL power optimization platform. It includes PowerPro CG (Clock Gating), PowerPro MG, PowerPro Analyzer including RTL power analysis capabilities, the PowerAdviser Flow, and SLEC Pro. Using the PowerPro platform, designers can significantly reduce power across an SoC design while reducing overall design time. PowerPro is the only RTL power optimization tool that integrates a complete formal equivalency checking flow, allowing users to confidently run the tool in a completely automatic manner.

PowerPro CG is an automated RTL power optimization tool that reduces power by up to 60 percent with little or no impact to timing or area. PowerPro CG reads in an RTL design and evaluates circuit behavior across

multiple clock cycles to identify sequential clock gating enable conditions. PowerPro CG then generates new low-power RTL that looks identical to the original RTL with the addition of sequential clock gating logic.

PowerPro MG is an automated memory power optimization solution that takes advantage of the low-power control options available in today's on-chip memories to reduce both dynamic and leakage memory power with little or no impact to timing or area. PowerPro MG reduces dynamic power by automatically generating logic to control the memory enable signal to eliminate unnecessary memory accesses. PowerPro MG reduces leakage power by automatically generating logic to control the sleep modes of individual embedded memories.

PowerPro Analyzer provides new RTL power analysis capabilities and complete visualization of PowerPro CG and PowerPro MG optimizations, allowing users to view power optimizations in the context of RTL source code, schematic display, sortable reports (ASCII, HTML, CSV, XML), and design hierarchy. PowerPro Analyzer is used in the PowerAdviser flow to provide the design and power information that designers can use to manually optimize their design.

SLEC Pro comprehensively verifies the power optimized RTL generated by PowerPro. SLEC Pro is a formal, functional sequential logic equivalence checker that ensures functional equivalence between the original RTL design and the corresponding power optimized RTL design for all possible input sequences.

Calypto at the Design Automation Conference (DAC)

Demonstrations of Calypto SLEC and PowerPro platforms are available during exhibit hours, Monday through Wednesday, 9am to 6pm, at Calypto's DAC booth #2012, San Diego Convention Center, San Diego, California. To request a private demo, please visit http://www.calypto.com/dac_registration.php.

About Calypto

Calypto Design Systems, Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class power optimization and functional verification software based on its patented Sequential Analysis Technology. Calypto, whose customers include Fortune 500 companies worldwide, is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor program, Si2, ARM Connections, and is an active participant in the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America. More information can be found at: www.calypto.com.

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Press Contact: Georgia Marszalek, ValleyPR LLC, _1 650 345 7477, Georgia@ValleyPR.com
Notes to editors: A graphic is available on request.