Calypto Announces Breakthrough Formal Verification Technology with Latest SLEC Release

SLEC 6.0 improves runtime performance by 5X; enhanced support for HLS flows

SANTA CLARA, CA – June 2, 2011 -- Calypto® Design Systems, Inc., the leader in sequential analysis technology, today announced version 6.0 of **SLEC®**, its Sequential Logic Equivalence Checking platform. The SLEC platform formally verifies Register Transfer Level (RTL) designs and system-level models without using testbenches or assertions. SLEC performs C to C, C to RTL and RTL to RTL equivalency checks, relieving the user from manually rewriting testbenches and re-running exhaustive regression simulations.

"SLEC has established itself as the only formal sequential equivalence checker for high level synthesis (HLS) flows, as well as for RTL-level sequential changes done by designers to close timing or power budgets," remarked Anmol Mathur, CTO, Calypto. "The enhancements in SLEC 6.0 significantly improve SLEC's capacity and expand its usage across all the different SLEC flows."

What's New in SLEC version 6.0

SLEC System HLS, which compares C models to automatically generated RTL models, improves interoperability by adding support for SystemC 2.2 and for all the supported vendors and their tools -Mentor Catapult, Cadence CtoS, Forte Cynthesizer. In addition, SLEC now has full integration and support for Catapult SystemC. The integration with CtoS has been enhanced with automatic inferencing of latency and throughput refinements, users no longer have to manually input this timing information. For Forte users, flow enhancements have been made involving external memory interfacing in pipelined designs.

SLEC System, which compares a C design to a manually written RTL design, has significant capacity improvements for the verification of IEEE compliant, floating point arithmetic designs. SLEC now comes with a native IEEE compliant C++ library, which is used as a reference model to equivalence check floating point RTL implementations, and a new Word-Level Solver architecture to enable efficient verification of floating point multipliers. Floating point RTL verification has been a significant pain point and often takes more than six months of simulation effort while suffering from low coverage. SLEC System reduces this effort from man months to man weeks. In addition, the usability of the manual flow offers significant enhancements with features such as an automatic wrapper and Tcl setup generation. These features cut the setup time for SLEC System by more than 3X.

SLEC Pro, which works in a completely integrated manner with Calypto's PowerPro Platform, has had significant runtime improvements, increasing performance by up to 5X when compared to its previous version. It also includes new formal verification techniques specifically targeted for the kind of power optimizations that are performed by PowerPro.

SLEC RTL, which compares two sequentially different RTL designs, has been enhanced to support complex clock and latch networks. In low level RTL design, the use of complex clocks and latches is very popular with high performance and low power microprocessor teams. This support enables SLEC RTL to be used across a wide range of blocks, making it the defacto solution for verifying embedded core optimizations at the RTL level.

Calypto at DAC

Demonstrations of Calypto SLEC and PowerPro platforms are available during Design Automation Conference exhibit hours, Monday through Wednesday, 9am to 6pm, at Calypto's DAC booth #2012, San Diego Convention Center, San Diego, California. To request a private demo, please visit http://www.calypto.com/dac_registration.php.

About Calypto

Calypto Design Systems, Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class power optimization and functional verification software, based on its patented Sequential Analysis Technology. Calypto, whose customers include Fortune 500 companies worldwide, is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor program, Si2, ARM Connected Community and is an active participant in the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America. More information can be found at: www.calypto.com.

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Notes to editors:
A graphic is available on request.