*NEWS RELEASE*

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# Calypto Delivers Industry's First Automated Tool for Memory Power Optimization

*PowerPro™ MG Enables system-on-a-chip (SoC) designers to produce the lowest power memory implementation possible*

**SANTA CLARA, Calif. — June 22, 2009 —** Enabling a breakthrough in automated system on a chip (SoC) design, Calypto® Design Systems Inc. (www.calypto.com) announced the availability of its PowerPro MG (memory gating) tool. The new tool is the industry's first product that automatically generates power-optimized RTL by taking advantage of the low-power modes available in today's leading on-chip memories. Employing a new "memory gating" technique, PowerPro MG eliminates costly and time-consuming manual coding. PowerPro MG will debut at this year's Design Automation Conference (DAC) in San Francisco.

"As a supplier to leading systems companies and seven out of the top 10 SoC providers, we are constantly challenged to deliver products that enable our customers to meet ever-tightening power budgets," said Tom Sandoval, chief executive officer of Calypto Design Systems. "Memory can account for up to 70 percent of the power consumed in an SoC. With PowerPro MG, designers can, for the first time, apply sequential analysis techniques to automatically generate memory gating logic that significantly reduces both static and dynamic on-chip memory power."

Currently, the design of logic used to control low-power memory modes requires hand-coding that is time-consuming and error-prone. By automatically generating logic to control low-power modes, PowerPro MG enables the lowest-power SoC possible and reduces that portion of the design cycle from weeks to hours.

Similar to its innovative PowerPro CG (clock gating) product, Calypto's PowerPro MG fits seamlessly into today's RTL synthesis flows. The tool reads in an RTL design written in VHDL or Verilog as well as the applicable memory models. Using Calypto's patented sequential analysis technology, the tool constructs new memory gating logic that works in conjunction with the low-power memory modes to produce the lowest power memory

implementation possible. PowerPro MG then generates new power-optimized RTL that looks identical to the original RTL except for the addition of the new memory gating logic. Aimed at large, complex SoC designs, PowerPro MG has been proven to reduce power consumption in a variety of end applications such as storage, networking, graphics and multimedia.

**Supports Leading Memory IP to Deliver Industry's Lowest Power Designs**

During the development of PowerPro MG, Calypto worked with Virage Logic, the semiconductor industry's trusted IP partner and leading embedded memory IP provider, to maximize the opportunity for memory power savings. "As the leader in RTL power optimization, Calypto is breaking new ground with the automation of a critical part of the SoC power optimization process," said Brani Buric, executive vice president, marketing and sales, of Virage Logic. "Using PowerPro MG in conjunction with Virage Logic's SiWare™ Memory products will help enable our customers to deliver designs that are as power-efficient as possible."

PowerPro MG works together with Calypto's PowerPro CG product to produce the lowest power design possible. PowerPro CG reduces power by implementing sequential clock gating logic in the non-memory portions of an RTL design. Calypto's SLEC product is used as part of a fully automated power optimization flow to comprehensively verify that the new power optimized RTL is functionally equivalent to the original RTL. Like PowerPro CG, the new PowerPro MG has no impact on the area or performance of a design.

"To achieve the lowest power implementations in today's complex SoCs, both static and dynamic power of logic and memory must be addressed. The flow must include multi-cycle sequential analysis for optimization and verification," said Dr. Gary Delp, VP and technical director of the Spirit Consortium and Co-Chair of the IEEE1801, Standard for Design and Verification of Low Power Integrated Circuits Committee. "Calypto's PowerPro family delivers an extremely effective and unique solution to SoC design teams."

**PowerPro MG Showcased at DAC 2009**

Highlighting its full suite of PowerPro and SLEC products, Calypto will demonstrate its new PowerPro MG product at this year's Design Automation Conference (DAC) in booth #1610, being held July 26-31 in San Francisco. To register for a private demonstration visit: www.calypto.com/events.php.

**Pricing and Availability**

Available now, Calypto's PowerPro MG runs on PC platforms running Linux and is priced at $295K for a one year time based license.

**About Calypto**

Founded in 2002, Calypto® Design Systems, Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class power optimization and functional verification software, based on its patented sequential analysis technology. Calypto, whose customers include Fortune 500 companies worldwide**,** is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor program, Si2 and is an active participant in the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America. Corporate headquarters is located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. More information can be found at: www.calypto.com.

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