NEWS RELEASE

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Calypto Enables ESL Design and Verification of Complex Designs with 5x Capacity Improvement

Improves HLS Tool Integration to Boost Designer Productivity, Adds Multiple Clock Support

SANTA CLARA, Calif. — July 20, 2009 — Enabling electronic system level (ESL) design flows for increasingly complex system on a chip (SOC) devices, Calypto® Design Systems Inc. (www.calypto.com) today announced the release of SLEC™ 4.0, the latest version of its popular sequential logic equivalence checking (SLEC) product family. SLEC is the semiconductor industry's only comprehensive functional verification solution that formally verifies equivalence between ESL models and RTL implementations. The new version has up to five times the capacity of the previous version and provides tighter integration with the leading high-level synthesis (HLS) tools from Cadence Design Systems, Mentor Graphics, and Forte.

"HLS tools are becoming more efficient at handling larger functions. As a result, customers are applying HLS tools to design blocks with significant complexity, especially from a sequential perspective," said Tom Sandoval, chief executive officer (CEO) of Calypto Design Systems. "SLEC 4.0 keeps pace with the most sophisticated designs and provides an automated path to comprehensive verification with the industry's only proven sequential equivalence checker. With SLEC, designers can avoid running time-consuming simulations and can uncover bugs that might otherwise go undetected and cause catastrophic delays to product development timelines."

Calypto pioneered sequential logic equivalence checking when it announced its first version of SLEC nearly five years ago. Since that time, SLEC's capacity has grown from thousand-gate blocks and tens of cycles of sequential complexity to hundreds of thousands of gates and thousands of cycles of sequential complexity. The verification challenges have increased exponentially with these more sophisticated functions, making traditional simulation-based verification even less effective.

Optimized Database and Improved Integration with HLS Tools

Featuring algorithmic enhancements to Calypto's patented word level solvers, the latest version of SLEC also includes dramatic improvement to SLEC's proprietary database that results in a reduced memory footprint while SLEC is running. Together, these advancements enable the tool to handle larger, more complex designs. As a result, designers can more freely use high level synthesis for the generation of highly complex functions, knowing that SLEC can provide comprehensive verification. The interface between SLEC and the leading HLS tools— Mentor Catapult, Cadence C-to-Silicon compiler, and Forte Cynthesizer —has also been improved in SLEC 4.0 to ensure an automated, efficient path to formal verification, requiring little or no user intervention.

Adds Multiple Clock Support

The ability to handle multiple clock designs has traditionally been a limitation with sequential logic equivalence checking. As SLEC capacity has increased, allowing the tool to support larger and more complex graphics, networking, multimedia, and wireless functions, the need to comprehensively verify designs with multiple clocks has become more and more prevalent. With version 4.0, SLEC customers can now fully verify designs with multiple, independent clocks. For example, SLEC RTL can verify that the relationship between two clocks (e.g. one clock is a multiple of another) is not disrupted by the manual introduction of sequential optimizations for power or performance by a designer. SLEC RTL can also now detect the illegal mixing of signals from different clock domains introduced by sequential transformations.

SLEC Family of Products

The SLEC family of products includes:

- **SLEC System**: Formally verifies equivalence of system-level models and RTL designs.
- **SLEC System-HLS**: Formally verifies that an RTL design generated using high-level synthesis is functionally equivalent to its corresponding system level model.
- **SLEC RTL:** Formally ensures functional equivalence between a golden RTL model and a corresponding RTL model has been sequentially modified to reduce power or improve performance.
- **SLEC Pro**: Comprehensively verifies that an RTL design generated by Calypto's PowerPro product is functionally equivalent to its corresponding golden RTL model.

SLEC 4.0 Showcased at 2009 DAC, Calypto to Present and Co-host Luncheon

Highlighting its full suite of PowerPro and SLEC products, Calypto will demonstrate its SLEC 4.0 at this year's DAC in booth #1610, being held July 26-31 in San Francisco. To register for a private demonstration visit: www.calypto.com/events.php.

Additionally, at DAC, Calypto speakers will present at the "Low-Power Coalition Workshop: Advances in Low-Power Design Throughout the Design Flow," at 3:30 p.m. on Sunday, July 26; at Cadence's "Eco-system booth" at 11:00 a.m. on Monday, July 27 and Wednesday, July 29; and at the "Non-cycle-accurate Sequential Equivalence Checking" session at 2:00 p.m. on Wednesday, July 29th.

Calypto will also co-host a luncheon presentation with Forte and Cadence on Tuesday, July 28 from 11:30a.m.-1:00p.m. "Are SystemC and TLM-based Design Ready to Replace RTL?" featuring industry leaders and moderated by Dr. Mark S. Johnstone, Freescale. To attend, visit: http://www.calypto.com/events.php.

Pricing and Availability

Available now, Calypto's SLEC 4.0 runs on PC platforms running Linux. Pricing for a one-year, time-based license is as follows:

SLEC System: $250,000

SLEC System-HLS (add on option to SLEC System): $50,000

SLEC RTL: $175,000

SLEC Pro: $125,000

About Calypto

Founded in 2002, Calypto® Design Systems, Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class power optimization and functional verification software, based on its patented sequential analysis technology. Calypto, whose customers include Fortune 500 companies worldwide**,** is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor program, Si2 and is an active participant in the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America. Corporate headquarters is located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. More information can be found at: www.calypto.com.

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