NEWS RELEASE

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Calypto Empowers Intrinsity to Deliver Industry's Fastest, Most Power-efficient Third-party Processor Cores

Comprehensive Verification Tool Enables Intrinsity to Aggressively Optimize Designs

SANTA CLARA, Calif. – November 23, 2009 – Calypto® Design Systems, the leader in sequential analysis technology, today announced that Intrinsity, Inc. is deploying Calypto's SLEC® RTL tool for the comprehensive verification of its products. Intrinsity implements industry-standard, cycle-accurate RTL cores from ARM®, PowerPC® and MIPS® in its Fast14® one-of-N domino logic to increase performance by as much as 65 percent, while maintaining low leakage and operating power characteristics in approximately the same silicon area.

"Calypto's SLEC RTL is critical to our design process because it is the only tool in the market that provides comprehensive verification of complex sequential optimizations," said Mark McDermott, general manager and vice president of engineering at Intrinsity. "It is an integral part of our verification methodology."

SLEC RTL, a sequential logic equivalence checker, enables designers to verify that the introduction of sequential optimizations such as clock gating, retiming and re-pipelining do not alter the functionality of designs. SLEC RTL also dramatically reduces the time, effort and cost associated with running extensive, resource-consuming simulation regressions.

"Innovative power and performance optimization techniques are the key differentiators for today's processor and DSP technology providers," said Tom Sandoval, CEO of Calypto Design Systems. "SLEC RTL provides designers at Intrinsity the confidence to use unconventional design methods to deliver substantially higher performance, lower power solutions."

About SLEC RTL

Used by leading system and IC companies worldwide, SLEC RTL comprehensively verifies that changes made to an RTL design do not impact functionality. By using formal techniques to compare the functionality of the original RTL design and the corresponding optimized RTL design for all possible input

sequences, SLEC RTL finds design errors that other tools miss. Unlike combinational equivalence checkers, SLEC RTL does not require one-to-one mapping of registers. SLEC is also able to take into account complex design schemes involving multiple clocks and intricate reset conditions. Using SLEC RTL, Intrinsity was able to implement design optimizations including RTL retiming to improve performance and clock gating to reduce power dissipation, and to comprehensively verify those optimizations without having to create complex test benches.

Pricing and Availability

SLEC RTL is available now and is priced at $175,000 for a one-year, time-based license.

About Calypto

Founded in 2002, Calypto Design Systems, Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class power optimization and functional verification software, based on its patented sequential analysis technology. Calypto, whose customers include Fortune 500 companies worldwide**,** is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor program, Si2 and is an active participant in the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America. Corporate Headquarters is located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. More information can be found at: www.calypto.com.

About Intrinsity

Intrinsity, Inc. is a design technology company that provides the designs, tools, technologies, and expertise so its customers can efficiently and predictably produce high performance, low-power and cost-effective products. Intrinsity's Fast14® technology is used to create FastCore® embedded cores, which provide not only circuit speeds greater than a GHz, but also the means to trade-off speed, power and area to achieve the optimal solution to customer design targets. Fast14® technology includes a combination of process specific libraries, a specification language and a set of tools that help automate the design flow. Intrinsity has a long history of designing high performance, low power semi-custom microprocessor cores that combine Fast14® NDL® (1-of-N Domino Logic) technology, custom SRAM, and synthesized static logic for ARM®, MIPS®, and PowerPC® cores. Its customers and strategic partners include ARM, AMCC, LSI Logic, and Samsung, among others. Intrinsity's corporate headquarters are located in Austin, Texas. For further information regarding Intrinsity, please visit our web site at http://www.intrinsity.com.

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