NEWS RELEASE

Calypto Extends Capabilities with Launch of SLEC CG for Verification of RTL Power Optimizations

Ability to Verify RTL Clock Gating Added to SLEC Product Family

SANTA CLARA, Calif. - November 6th, 2006 - Calypto™ Design Systems Inc. the leader in sequential analysis technology, today launched SLEC™ CG (Sequential Logic Equivalence Checking for Clock Gating), software for verifying register transfer level (RTL) power optimizations.

SLEC CG is the latest addition to the SLEC product family, the semiconductor industry's only sequential logic equivalence checking solution that can verify functional equivalence between designs with sequential differences including RTL clock gating changes. SLEC CG functionally verifies RTL power optimizations without the need for writing specific testbenches or running simulation.

Introducing SLEC CG

SLEC CG quickly identifies design bugs, reducing verification effort to a fraction of what is required when using traditional simulation methods. By formally verifying RTL clock gating changes, SLEC CG is able to find elusive corner-case bugs and provide designers an efficient, block-level debug environment.

SLEC CG automatically detects clock-gating logic and validates that the enabling logic is stable in relation to the clock edge. SLEC CG verifies all possible input sequences that enable and disable clocks, as well as complex clock gating schemes that cross hierarchies and block boundaries – conditions that can be hard to control and observe with testbench-driven verification.

"Power is the primary concern for today's SOC designs," explains Tom Sandoval, Calypto's chief executive officer. "SLEC CG gives design teams a way to confidently verify aggressive RTL power optimization, ensuring their original design functionality has not changed."

Pricing and Availability

SLEC CG is available immediately and supports VHDL and Verilog. Design teams with existing licenses will receive SLEC CG as part of their SLEC RTL and SLEC System products. SLEC CG runs on Linux operating systems and is priced from $125,000 (U.S. pricing). For more details, contact Mitch Dale, Calypto's Product Marketing Director, at (408) 850-2339 or mdale@calypto.com.

About Calypto

Founded in 2002, Calypto Design Systems, Inc. enables SoC design teams to bridge System and RTL for semiconductor design, thereby saving millions of dollars in design costs and silicon re-spins. It delivers software products to leading edge semiconductor and systems companies worldwide. Calypto is privately held with venture funding from Cipio Partners,

JAFCO Ventures, Tallwood Venture Capital and Walden International. It is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, and the Mentor Graphics OpenDoor program. Corporate Headquarters are located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. Email: calypto_info@calypto.com. More information about Calypto may be found at: http://www.calypto.com

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