NEWS RELEASE

Calypto Design Systems Reveals Strategy to Bridge System and RTL Design
Company targets both RTL and system-level design and verification needs

SANTA CLARA, Calif., January 17, 2005 - Calypto Design Systems, Inc. today unveiled its strategy for bridging the gap between electronic system level design and integrated circuit (IC) implementation. The company intends to broadly deploy electronic design automation (EDA) products based on unique, proprietary technology that will connect system-level models and register transfer level (RTL) design flows in order to support faster verification times and design at a higher level of sequential abstraction. The company strategy will focus and address on the needs of both system-level designers and RTL-designers.

Founded in 2002 by a team of EDA and IC design veterans, Calypto has already raised more than $22 million in Series A and Series B funding from premiere firms such as Infineon Ventures, JAFCO Ventures, Tallwood Venture Capital, and Walden International. The company has a veteran board of outside directors including George Pavlov, general partner of Tallwood Venture Capital, Lip-Bu Tan, chairman of Walden International, and Albert Yu, former Intel SVP and private investor.

"Today, the process of ensuring that a complex chip design will match its functional system requirements is among the most time-consuming, expensive, and fallible processes that chip design teams go through," stated Mahesh Balakrishnan, Managing Director of Infineon

Ventures N.A. "Calypto has a unique grasp on the issues and challenges that design teams are wrestling with. We made the investment in them because we believe that they have the vision, team, and technology to address these challenges."

"In connecting system-and-RTL design into a single continuum, the Calypto team is addressing a difficult and substantial industry challenge," stated Bruce Beers, former vice president at IBM Microelectronics and member of the Calypto Advisory Board. "Delivering on their vision will have a dramatic impact on the overall design process."

Enabling the System-to-RTL Continuum

A complex IC today contains more than one million lines of RTL code that must be verified against functional requirements. This code is constantly changing through the design process as designers target aggressive power consumption and timing constraints, and must be re-verified through these multiple iterations. This functional verification is consuming up to 75% of total design time and resources. Yet, an estimated 45% of all design starts require multi-million dollar silicon re-spins because of undetected functional bugs. The fastest way to find functional errors and verify system requirements is to design and verify at a higher level of abstraction.

Regardless of whether design teams have already adopted a system-level design flow, the teams are already moving up in abstractions. To meet power or timing goals, design teams make micro-architectural refinements (such as retiming, pipelining, state re-encoding and resource sharing) to their designs. These refinements change the sequential nature of the original designs, and thereby move up in a sequential level of abstraction from a pure RTL level.

These changes have not been well-supported by a standard EDA design flow. There has been no easy way for design teams to know which sequential changes to make, to know how to perform and automate these changes, and most importantly -- no easy way for design teams to ensure functional equivalency as they make these sequential changes.

"Today, design and verification teams must make a leap of faith when they move to a higher level of design abstraction - or when they move from system-level verification models to RTL. The semiconductor industry has a growing need for EDA solutions that will simplify the design flow while enabling designers to move to higher levels of sequential abstraction," stated Devadas Varma, CEO of Calypto. "There has been no good, automated connection that allows design and verification teams to move between different levels of sequential abstraction. Our technology solves this problem."

Calypto will deliver unique technology that enables teams to design and verify at a higher level of abstraction. This technology will support a System-to-RTL continuum which allows users to easily navigate between various levels of abstraction in order to make system-level or micro-architectural changes to a design, quickly verify them, and then retarget the design towards an RTL implementation flow.

The company intends to commence its first broad scale product release in second quarter of 2005.

About Calypto

Founded in 2002, Calypto Design Systems enables IC design teams to bridge the system-to-RTL design gap, thereby saving millions of dollars in design costs and silicon re-spins. The

company delivers software products to leading edge semiconductor and systems companies worldwide. Calypto is privately held, with venture funding from Infineon Ventures, JAFCO Ventures, Tallwood Venture Capital and Walden International. The company is a member of the Cadence Connections program, IEEE-SA, the Open SystemC Initiative (OSCI), Synopsys SystemVerilog Catalyst Program, and has an ongoing alliance with the Model Technologies group of Mentor Graphics. More information about the company may be found at www.calypto.com.

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