NEWS RELEASE

Calypto's SLEC™ RTL Product Selected by AMD to Verify Advanced Processors
Calypto's SLEC Used to Verify RTL Clock Gating Optimizations and Catch Hard-to-Detect Bugs

SANTA CLARA, Calif. - March 14th, 2007 - Calypto™ Design Systems Inc. the leader in sequential analysis technology, announced today that AMD (NYSE:AMD), has adopted its Calypto's SLEC™ (sequential logic equivalence checking) product into its microprocessor design flow.

AMD chose SLEC RTL software to verify performance and power optimizations in its advanced microprocessor design flow.

The SLEC RTL product comprehensively verifies sequential optimizations, such as RTL retiming and clock gating which are typically performed in microprocessor design flows. SLEC uncovers design differences in short concise waveforms, simplifying error detection and reducing debug time from weeks to days.

"Our microprocessor design teams are consistently innovating to increase overall performance and deliver industry-leading performance-per-watt," says Nihar Mohapatra, design verification lead, AMD. "The fast, comprehensive verification which Calypto's SLEC provides enhances this creative process, helping our design teams continue to meet the processing needs of our customers."

AMD's leading-edge processors feature AMD's Direct Connect Architecture, which helps eliminate the bottlenecks inherent in a front-side bus by directly connecting the processors, the memory controller and the I/O unit to enable improved overall system performance and power efficiency. The AMD Opteron processor is the only x86 server processor with planned upgradeability to native quad-core within the same thermal design power envelope. Upcoming native Quad-Core AMD Opteron processors (codenamed "Barcelona") are estimated to provide a 40-percent performance advantage over the competition, and will enable new power- and thermal-management techniques, strengthening the industry-leading performance-per-watt AMD Opteron processors currently deliver today.

SLEC is the semiconductor industry's only Sequential Logic Equivalence Checking solution that can verify functional equivalence between designs with sequential differences. Also part of the SLEC product family is SLEC System, which verifies that RTL implementations functionally match System level models written in SystemC or C/C++. The SLEC product family is based on unique sequential analysis technology that bridges levels of design abstraction, Enabling ESL™.

Commenting on SLEC's success and market adoption, Tom Sandoval, Calypto's Chief Executive Officer remarks: "It has become extremely difficult to meet both power and performance targets using traditional gate-level methods. To achieve design goals, hardware engineers must make micro-architectural changes to their RTL. Using SLEC, design teams can create higher quality designs in less time."

About Calypto

Founded in 2002, Calypto Design Systems, Inc. enables SoC design teams to bridge System and RTL for semiconductor design, thereby saving millions of dollars in design costs and silicon re-spins. It delivers software products to leading edge semiconductor and systems companies worldwide. Calypto is privately held with venture funding from Cipio Partners, JAFCO Ventures, Tallwood Venture Capital and Walden International. It is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, and the Mentor Graphics OpenDoor program. Corporate Headquarters are located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. Email: calypto_info@calypto.com. More information about Calypto may be found at: http://www.calypto.com

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