NEWS RELEASE

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Calypto Releases PowerPro CG 2.0
Additional Power Savings,Graphical Power Analyzer
Broaden PowerPro CG's Application for Storage, Processor Markets

SANTA CLARA, Calif. — March 24, 2008 — Calypto™ Design Systems Inc., the leader in sequential analysis technology, announced today immediate availability of PowerPro™ CG 2.0 featuring new sequential clock-gating optimizations that extend its power savings capability to a wider range of design applications in the storage and processor markets. Additionally, the 2.0 release includes PowerPro Analyzer, a graphical visualization tool with hyperlinked source code, schematics and clock-gating views that enable users to rapidly navigate and analyze power optimizations.

"With the additional sequential power optimizations and new capabilities in PowerPro CG 2.0, Calypto is delivering the power savings our customers need to meet the requirements of today's advanced, low-power electronic systems," says Tom Sandoval, Calypto's chief executive officer. "This release benefits our existing customers and extends our reach into the power-sensitive storage and processor markets."

PowerPro CG is an automated Register Transfer Level (RTL) power optimization product that reduces power consumption in typical system-on-chip (SoC) devices by 10% to

60% with little or no impact on timing or area. It delivers consistently better results in significantly less time than the error-prone and time-consuming manual techniques currently used by designers.

PowerPro CG uses Calypto's patented sequential analysis technology to evaluate circuit behavior across multiple clock cycles and identify sequential clock gating logic to reduce dynamic power. PowerPro CG then inserts this logic into the user's original synthesizable RTL code, while maintaining all of the original RTL constructs including any existing pragmas and comments. Compared to combinational clock gating, sequential clock gating saves more power by turning off a larger number registers for longer durations.

New sequential clock gating optimizations in PowerPro CG 2.0 exploit the type of control and data interactions typically found in storage and processor designs. PowerPro CG 2.0 is easily integrated into low-power RTL synthesis design flows. Calypto's SLEC™ (for Sequential Logic Equivalence Checker) product is integrated with PowerPro CG to comprehensively verify sequential clock-gating optimizations.

Availability and Pricing

PowerPro CG 2.0 is available now, runs on x86/Linux platforms and is priced at $295,000 (U.S. dollars) for a one year time-based license.

To learn more, visit the Calypto website at http://www.calypto.com.

About Calypto

Founded in 2002, Calypto Design Systems, Inc. enables SoC design teams to bridge System and RTL for semiconductor design, saving millions of dollars in design costs and silicon re-spins. Enabling ESL, Calypto delivers software products to leading-edge semiconductor and systems companies worldwide. Calypto is a member of the Cadence

Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program and the Mentor Graphics OpenDoor program. Corporate Headquarters is located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. More information about Calypto may be found at: http://www.calypto.com.

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