NEWS RELEASE

Calypto Debuts Sequential Power Optimization Solution for Automated RTL Power Reduction

PowerPro CG Reduces Power Consumption by up to 60% allowing Design Teams to Lower System Costs, Reduce Design Time and Extend Battery Life

SANTA CLARA, Calif. - March 26th, 2007 - Calypto™ Design Systems Inc., the leader in sequential analysis technology, today announced the immediate availability of PowerPro™ CG, which has reduced power by up to 60% on initial customer designs with no impact on functionality, area or performance.

PowerPro CG -- for PowerPro Clock Gating -- dramatically reduces power consumption by applying sequential analysis at the register transfer level (RTL) to identify micro-architectural optimizations that result in a lower power circuit.

By analyzing the sequential behavior of synthesizable RTL across multiple clock cycles, PowerPro CG identifies regions of a chip that can be clock gated to reduce dynamic power. It then automatically generates the clock-gating enable logic, providing consistently better results in significantly less time than the error prone, time consuming manual techniques used by design teams today.

"RTL power optimization is a critical step in our high-performance, low-power design methodology for PC graphics, visual computing and applications processors," said Dan Smith, Director, Hardware Engineering, NVIDIA Corporation. "PowerPro CG has shown substantial

power savings on designs, including blocks already manually optimized for low power by RTL designers."

Unlike combinational power reduction tools, PowerPro CG identifies and generates sequential clock-gating transformations. By fitting into existing design flows with industry standard library, timing, and switching activity file formats, the power savings achieved by PowerPro CG are complementary and cumulative to optimizations performed by synthesis and placement tools downstream.

Introducing the PowerPro Product Family

PowerPro is Calypto's latest offering based on the company's unique sequential analysis technology. The clock-gating capabilities in PowerPro CG incorporate power optimization engines with concurrent area, timing, and power analysis to enable a variety of clock-gating transformations that reduce dynamic power without negatively impacting leakage power. PowerPro CG, the first product released in the PowerPro family, specifically targets the automation of sequential RTL clock-gating optimization.

"PowerPro CG is a breakthrough product in the Electronic Design Automation market," said Tom Sandoval, Chief Executive Officer of Calypto. "For our customers, achieving the lowest possible power consumption is a true competitive advantage, and sequential clock-gating at the RTL level is a critical step in achieving that goal."

Availability and Pricing

PowerPro is available now and runs on PC platforms running Linux. It is priced at $295,000 (U.S. dollars) for a one year time-based license.

For more details, visit the Calypto website at http://www.calypto.com or contact Mitch Dale, Calypto's product marketing director, at (408) 850-2339 or via email at mdale@calypto.com.

About Calypto

Founded in 2002, Calypto Design Systems, Inc. enables SoC design teams to bridge System and RTL for semiconductor design, saving millions of dollars in design costs and silicon re-spins. It delivers software products to leading edge semiconductor and systems companies worldwide. Calypto is privately held with venture funding from Cipio Partners, JAFCO Ventures, Tallwood Venture Capital and Walden International. It is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program and the Mentor Graphics OpenDoor program. Corporate Headquarters is located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. Email: calypto_info@calypto.com. More information about Calypto may be found at: http://www.calypto.com

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