NEWS RELEASE

Calypto Pioneers Breakthrough Verification Technology

Industry's first sequential equivalence checker enables new generation of functional verification

SANTA CLARA, Calif. - April 25, 2005 - Calypto Design Systems, Inc. today introduced its SLEC™ product family -- the semiconductor industry's only sequential logic equivalence checking solution. The SLEC family delivers dramatic improvement in integrated circuit (IC) functional verification, offering design teams increased productivity, confidence and flexibility in making changes to meet their IC power and performance goals.

"The semiconductor industry is moving to the next level of design productivity by embracing higher levels of abstraction," stated Devadas Varma, CEO of Calypto. "For design teams to realize the advantages of system-level design they must have tools to quickly verify that RTL implementations match system-level specifications. We developed the SLEC product family to address this critical need."

The SLEC product family is the first commercially available platform that proves functional equivalence between two IC designs that contain differences in levels of abstraction and sequential behavior. SLEC can verify designs with sequential differences such as micro-architectural changes, state machine modifications, timing re-balancing, and interface differences. The SLEC sequential equivalence checking software is based on a patent-pending

hybrid verification technology that, unlike traditional combinational equivalence checkers, can support designs with sequential differences.

"SLEC's ability to verify sequential differences is a strong addition to our advanced verification methodology," said Osamu Tada, department manager of System Level Design and Verification Technology Dept., LSI Product Technology Unit at Renesas Technology Corp. "It offers us an innovative approach for functional verification as we refine our design at various levels of abstraction. We consider SLEC an important tool in our high-level design flow."

The SLEC product family initially includes two products: SLEC SYSTEM and SLEC RTL. SLEC SYSTEM is used by design teams to check that RTL implementations match a system-level design, while SLEC RTL checks functional equivalence between two versions of an RTL design that have dramatically different architectures and timing.

Supporting the System-to-RTL Continuum

Moving to high level design is a process of navigating the System-to-RTL continuum. A continuum approach is required for design teams to work at multiple levels of sequential and data abstraction -- from fully-timed RTL implementation to transaction-level modeling. SLEC allows designers to navigate the System-to-RTL continuum by verifying functional equivalence across levels of sequential and data abstraction.

Design teams who adopted system-level design methodologies can use the SLEC products to leverage their investment in system-level validation to verify and refine RTL implementations. SLEC enables designers to quickly verify RTL refinements without having to spend time running a full regression suite. Likewise, RTL designers can leverage previously

validated designs to confidently make sequential changes such as pipelining and resource sharing that would have previously taken weeks of simulation time to verify. In both cases, the SLEC platform delivers a comprehensive sequential verification solution that identifies bugs that are difficult to find or missed when using traditional simulation methods. With SLEC, design teams quickly detect side effects that have been introduced during block-level optimization. This gives engineers more freedom in the design options they have, dramatically improving design efficiency.

Calypto will be hosting demonstrations of the SLEC product family in booth #1818 at the 42nd annual Design Automation Conference taking place in the Anaheim Convention Center from June 13 - 16, 2005. To register for demonstration slots, please visit www.calypto.com.

Pricing and Availability

The SLEC product family is immediately available with support for Verilog, VHDL, SystemC and C/C++ hardware descriptions. Pricing for SLEC products begin at $175,000 for a one year floating license on Linux platforms.

About Calypto

Founded in 2002, Calypto Design Systems, Inc. enables IC design teams to bridge the system-to-RTL design gap, thereby saving millions of dollars in design costs and silicon re-spins. The company delivers software products to leading edge semiconductor and systems companies worldwide. Calypto is privately held with venture funding from Cipio Partners, JAFCO Ventures, Tallwood Venture Capital and Walden International. The company is a

member of the Cadence Connections program, the IEEE-SA, the Open SystemC Initiative (OSCI), Synopsys SystemVerilog Catalyst Program, and has an ongoing alliance with the Model Technologies group of Mentor Graphics. More information about the company may be found at www.calypto.com.

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