NEWS RELEASE

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Calypto to Offer Power Profiling Software Free of Charge at DAC
Calypto's Power, Verification Experts to Demonstrate Products, Participate in DAC Technical Program

Santa Clara, Calif. — May 21, 2008 **—** Calypto™ Design Systems Inc., the leader in sequential analysis technology, will offer qualified Design Automation Conference (DAC) attendees who visit the Calypto Booth (#1354) a free copy of PowerPro-filer on a one gigabyte memory stick.

The recently introduced PowerPro-filer is a Linux program that reads synthesizable Verilog code and reports how well a register transfer level (RTL) design is optimized for power by providing designers with *Clock-Gating Efficiency* statistics. *Clock-gating Efficiency* correlates directly to how well a designer's clock gating implementation impacts dynamic power.

Calypto's technical experts will be on hand at DAC in Booth 1354 June 9-12 at the Anaheim Convention Center in Anaheim, Calif. They will demonstrate how Calypto's customers have dramatically reduced power and improved design quality using PowerPro™ CG (clock gating) for automated RTL power optimization and SLEC™ (Sequential Logic Equivalence Checker) for functional verification.

To register for a private demonstration, visit: www.calypto.com/events.php.

Additionally, Calypto is featured throughout the DAC technical program. Several of its power and verification experts will participate in technical sessions, including:

- The panel "Keeping Hot Chips Cool: Are IC Thermal Problems Hot Air?," moderated by Devadas Varma, chairman and founder. It will be held Wednesday, June 11, from 4:30-6 p.m. in room 210CD.

- The special session titled, "Formal Verification, Dude or Dud? Experience from the Trenches," led by Anmol Mathur, chief technology officer and founder. It will be held Thursday, June 12, from 2- 4 p.m. in room 207.

- "Leveraging Sequential Equivalence Checking to Enable System-level to RTL Flows," will be presented during this session by Pascal Urard of STMicroelectronics. It was co-authored by Venkatram Krishnaswamy, vice president of application engineering and services.

- The technical paper "Construction of Concrete Verification Models from C++," presented by Malay Haldar, senior engineering manager. This is part of a session titled, "Advances in Verification of Abstract (pre-RTL)," to be held Thursday, June 12, from 4:30-6 p.m. in room 208AB.

Calypto's products — based on its patented sequential analysis technology — include the SLEC product family that provides comprehensive functional verification and the PowerPro product family that reduces power by up to 60% in RTL designs.

SLEC is an industry proven sequential equivalence checker that handles differences in design state, timing and levels of abstraction. SLEC System *Enables ESL*™ by comprehensively verifying RTL implementations using electronic system level (ESL) models.

PowerPro CG is an automated RTL power optimization product that identifies and inserts sequential clock gating enable logic into synthesizable Verilog and VHDL designs.

About Calypto

Founded in 2002, Calypto Design Systems, Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class power optimization and functional verification software, based on its patented sequential analysis technology. Calypto, whose customers include Fortune 500 companies worldwide**,** is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program and the Mentor Graphics OpenDoor program. Calypto has offices in Europe, India, Japan and North America. Corporate Headquarters is located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. More information can be found at: www.calypto.com.

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