# *NEWS RELEASE*

**Calypto Expands Sequential Analysis Capabilities with SLEC 2.0 Release**
*New Features And 100x Increased Capacity Enable Broad Base ESL Growth*

**SANTA CLARA, Calif. - May 22nd, 2006 -** Calypto™ Design Systems, Inc. today released version 2.0 of its SLEC™ product family, the semiconductor industry's only sequential logic equivalence checking solution that can verify functional equivalence between a System-Level model and its corresponding RTL model independent of sequential differences.

SLEC 2.0 increases capacity by 100x for System Level designs over previous releases, dramatically improves runtime and further simplifies the design debug process with counter example enhancements. This new technology provides the capabilities required for the broad electronic system level (ESL) market.

"Our advanced System-Level Flow provides significant benefit to the designers of the world's most complex image processing and digital communications products," states Pascal Urard, High Level Synthesis Manager at STMicroelectronics. "SLEC 2.0 allows us to design blocks of several hundred thousand gates at a higher level of abstraction by keeping all the various models in sync at all stages of development."

"Today's SoC Designers need to move to system level design to drive innovation and enhance their competitive advantage," says Tom Sandoval, chief executive officer (CEO) of Calypto Design Systems. "SLEC 2.0 is the only technology that enables designers to bridge a

System-Level model to its equivalent RTL implementation, independent of sequential differences. It is the key technology that is enabling ESL."

The foundation of sequential analysis is the ability to deal with large, complex changes in design state and abstraction. In SLEC 2.0, Calypto has extended its unique, patented sequential analysis engine with a new algorithm that gives a 100x improvement in handling sequential changes. Sequential changes are common when comparing functional system-level designs with cycle accurate RTL designs. SLEC 2.0 can handle designs where the state and temporal differences are measured in the millions.

Design teams who adopt system-level design methodologies can use the SLEC products to leverage their investment in system-level validation to verify and refine RTL implementations. SLEC enables designers to quickly verify RTL refinements without having to spend time and resources running a full regression suite. Likewise, RTL designers can leverage previously validated designs to confidently make sequential changes such as pipelining and resource sharing for power and performance improvement that would have previously taken weeks of simulation time to verify. In both cases, the SLEC platform delivers a comprehensive sequential verification solution that identifies bugs that are difficult to find or missed when using traditional simulation methods.

"A broad spectrum of IC designers in the communications, wireless and consumer markets can now rapidly verify micro-architecture changes made to an RTL implementation model to optimize power and performance," adds Sandoval. "SLEC 2.0 ensures comprehensive functional equivalence to the corresponding system-level model, dramatically reducing the need to run time consuming, exhaustive simulations."

SLEC will be demonstrated during the 43rd Design Automation Conference (DAC) July 24-27 at the Moscone Center in San Francisco in Booth #628.

**Pricing and Availability**

The SLEC 2.0 product family is immediately available with support for Verilog, VHDL, SystemC and C/C++ hardware descriptions. It runs on Linux operating systems and is priced from $175,000.

For more details, contact Calypto at info@calypto.com.

**About Calypto**

Founded in 2002, Calypto Design Systems, Inc. enables SoC design teams to bridge system and RTL for semiconductor design, thereby saving millions of dollars in design costs and silicon re-spins. The company delivers software products to leading edge semiconductor and systems companies worldwide. Calypto is privately held with venture funding from Cipio Partners, JAFCO Ventures, Tallwood Venture Capital and Walden International. The company is a member of the Cadence Connections program, the IEEE-SA, the Open SystemC Initiative (OSCI), Synopsys SystemVerilog Catalyst Program, and the Mentor Graphics OpenDoor program. Corporate Headquarters are located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. Facsimile: (408) 850-2301. Email: info@calypto.com. More information about the company may be found at www.calypto.com.

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