NEWS RELEASE

For more information, contact:
Nanette Collins
Public Relations for Calypto Design Systems
(617) 437-1822
nanette@nvc.com

Calypto Delivers Optimized Power Flow with Cadence Design Systems

Power optimization flow reduces power consumption without compromising performance

SANTA CLARA, CALIF. — May 23, 2008 — Calypto™ Design Systems Inc., the leader in sequential analysis technology, today announced the availability of an RTL power optimization flow to integrate Calypto's PowerPro CG product with the Encounter® RTL Compiler from Cadence Design Systems, Inc. The integrated flow provides an automated, single-pass sequential analysis capability that produces the lowest power implementation while still meeting design constraints.

By using Encounter RTL Compiler's multi-objective synthesis and PowerPro CG's sequential analysis capability, the integrated flow optimizes sequential clock gating by using accurate timing information in the power/performance trade-off analysis. The collaborative effort has resulted in a seamless design flow that generates RTL code that reduces power in system-on-chip designs. In addition, the collaboration has identified new constructs to be added to the Si2 Common Power Format (CPF) standard that will be beneficial for system-level design flows.

"The integration of PowerPro CG with Encounter RTL Compiler provides our mutual customers with automated sequential RTL clock gating within their existing synthesis environments," adds Nimish Modi, corporate vice president of Front-End Design R&D at Cadence. "This provides customers with additional power optimization while not impacting the performance of their designs."

Calypto's PowerPro CG which is based on patented Sequential Analysis Technology reduces power by up to 60%. PowerPro CG evaluates circuit behavior across multiple clock cycles to identify and insert sequential clock gating enable logic into RTL designs while maintaining all user defined pragmas and comments. PowerPro CG consistently produces better results in significantly less time than manual clock gating.

The Cadence Encounter® RTL Compiler, a key technology in the Cadence® Encounter digital IC design platform and a component of the Cadence Logic Design Team Solution, delivers production-proven global synthesis for faster, smaller, and low-power chips in less time. With its unique set of patented global-focus algorithms, combined with physically-aware optimization and analysis, Encounter RTL Compiler cuts design time while ensuring the highest quality of silicon.

"We are delighted to work with Cadence and the Power Forward Initiative to deliver this industry leading RTL power optimization flow," remarks Tom Sandoval, Calypto's chief executive officer (CEO). "We will continue to work with the Power Forward Initiative to define new ways to improve low-power design flows that produce the lowest power SoC's possible."

CPF, a Si2 standard format, is used for specifying power-saving techniques early in the design process, enabling sharing and reuse of low-power intelligence throughout the

design flow. The Cadence Low-Power Solution is the industry's first complete flow that integrates logic design, verification, and implementation with the Common Power Format.

About Power Forward Initiative

The Power Forward Initiative, which has more than 25 member companies, is an industry initiative sponsored by Cadence and has the goal of enabling the design and production of more power-efficient electronic devices. The initiative includes companies representing a broad cross section of the design chain including system, semiconductor, foundry, IP, EDA, ASIC and design services companies. CPF was contributed by Cadence to the Si2 Low-Power Coalition in December 2006 and CPF 1.0 is now available as an Si2 standard to the industry at large. The Initiative has also published *A Practical Guide to Low-Power Design — User experience with CPF* which is aimed at educating the broad design marketplace in utilizing advanced low-power design techniques. The Guide is available free of charge at www.powerforward.org.

About Calypto

Founded in 2002, Calypto Design Systems, Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class power optimization and functional verification software, based on its patented sequential analysis technology. Calypto, whose customers include Fortune 500 companies worldwide**,** is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor program and the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America. Corporate Headquarters is located at: 2933

Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. More information can be found at: www.calypto.com.

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