NEWS RELEASE

Calypto and Mentor Graphics Integrate Tools for Verifiable, Automated Path from System to RTL

Calypto joins Mentor OpenDoor® program

SANTA CLARA, Calif. - June 2, 2005 - Calypto Design Systems, Inc., the technology leader bridging system and register-transfer-level (RTL) design today announced plans to collaborate with Mentor Graphics to integrate the Calypto SLEC™ sequential equivalence checker with Mentor Graphics' Catapult™ C Synthesis tool, providing integrated circuit (IC) designers with a joint, verifiable, automated flow from an algorithmic chip description to an RTL description. The companies will demonstrate this flow at the Design Automation Conference, June 13 - 17th. To support these activities, Calypto has become a member of the Mentor Graphics OpenDoor® partnership program.

With this integration, Catapult C users can automatically generate RTL from a pure ANSI C/C++ description, then automatically create SystemC ' wrappers' containing verification directives and an interface mapping directly into the SLEC environment. This allows users to quickly verify functional equivalence between the pure ANSI C/C++ and RTL descriptions and quickly verify additional design optimizations before handing off to final integrated circuit implementation.

"Design teams today are moving towards higher levels of abstraction in the design process - yet they require a fast and effective way to gain confidence that their RTL matches the system-level description," stated Michael Sanie, vice president of marketing and business development at Calypto Design Systems. "The integration of Catapult C with Calypto' s SLEC will give them a path to safely and quickly navigate the system-to-RTL continuum."

"SLEC offers a very innovative approach which promises to dramatically improve verification for ESL synthesis flows," stated Shawn McCloud, high-level synthesis product manager, Mentor Graphics Corporation. "By connecting Catapult C Synthesis, the only pure ANSI C++ synthesis tool, with sequential equivalence checking technology from Calypto, we are jointly providing users a safe, verifiable flow from Algorithmic C++ to RTL for both ASIC and FPGA technologies"

The companies will be showing a joint demonstration of this flow in the Calypto Suite - at booth #1818. To register for a demo, see www.calypto.com.

About Calypto

Founded in 2002, Calypto Design Systems, Inc. enables IC design teams to bridge system and RTL for semiconductor design, thereby saving millions of dollars in design costs and silicon re-spins. The company delivers software products to leading edge semiconductor and systems companies worldwide. Calypto is privately held with venture funding from Cipio Partners, JAFCO Ventures, Tallwood Venture Capital and Walden International. The company is a member of the Cadence Connections program, the IEEE-SA, the Open SystemC Initiative

(OSCI), Synopsys SystemVerilog Catalyst Program, and the Mentor Graphics OpenDoor program. More information about the company may be found at www.calypto.com.

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