*NEWS RELEASE*

Calypto DAC Booth #1610

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# Calypto Delivers Fully Automated Sequential Optimization Flow for High-performance IP Blocks

*PowerPro CG, SLEC RTL Combine with Popular Synthesis Tools to Achieve Power, Performance and Area Goals*

**SAN FRANCISCO — July 27, 2009 —** Calypto® Design Systems Inc. (www.calypto.com), the leader in sequential analysis technology, today announced a fully automated design flow aimed at advancing the delivery of optimized, high-performance IP blocks found in today's leading SoC designs. Enabled by Calypto's SLEC RTL tool and new analysis capabilities in its proven PowerPro CG (clock gating) tool, Calypto's Sequential Optimization Flow allows designers, for the first time, to use a fully automated flow to optimize power, area, and timing for high-performance IP blocks, such as microprocessors and digital signal processors (DSPs). Using the flow, designers are also assured that functionality is maintained throughout the process. Calypto will demonstrate its Sequential Optimization Flow this week at its booth during the 2009 Design Automation Conference (DAC) held in San Francisco.

"With each new generation of electronics products, SoC designers are challenged to deliver higher performance functions that dissipate less power and occupy less silicon area than the previous generation," said Tom Sandoval, CEO of Calypto. "We have developed an automated flow that dramatically reduces the design time and resources required to deliver low-power, high-performance, differentiated functionality. As a result, even small SoC design teams are enabled to efficiently meet their strict power, performance and area goals using an automated method that includes proven tools for both optimization and comprehensive verification."

Without an automated approach, design teams have been forced to engage in manual optimizations that can be costly, time consuming and error prone. This process frequently results in timing issues which, in turn, lead to increased circuit area and power consumption. Moreover, manual optimizations require extensive resources and unique skill sets, making the process off-

limits to smaller design teams. Calypto's new Sequential Optimization Flow addresses these challenges.

**New Flow Targets Retiming Synthesis Functionality with Automated Analysis**

Calypto's new Sequential Optimization Flow includes PowerPro CG, which takes an RTL design and automatically generates a power-optimized RTL design. Both the original and power-optimized RTL designs are run through a third-party synthesis tool, such as the Encounter® RTL Compiler from Cadence Design Systems, Inc., to create two gate-level netlists. With the new automated analysis capabilities of PowerPro CG, the timing and power consumption of both netlists are automatically analyzed so that targeted retiming synthesis can be run on the power-optimized, gate-level netlist. Using Calypto's SLEC RTL, functional equivalence between the original RTL and the new timing- and power-optimized gate level netlist is verified. By combining gate-level retiming with automated RTL power optimization and sequential logic equivalence checking, Calypto's Sequential Optimization Flow enables SoC design teams to optimize power, area and timing for IP blocks and complex functions that were previously considered off-limits to such optimizations.

**New Sequential Optimization Flow Showcased at the 2009 DAC**

Calypto is showcasing the results of running the Sequential Optimization Flow on the Sun Microsystems OpenSPARC T1 processor core at the 2009 DAC. Sun has made this 64-bit, high-throughput, low-power core available to the public under the GNU v2.0 license. Calypto will demonstrate how running the core through the flow results in a 24 percent power advantage and almost five percent area advantage over the original core, with no performance impact. DAC attendees will see, firsthand, the effectiveness of the flow. Details of the Sequential Optimization Flow and the results of using the flow on the OpenSPARC core will be provided.

Calypto will also demonstrate its full suite of PowerPro and SLEC products at this year's DAC in booth #1610, being held July 26-31 in San Francisco at the Moscone Center. To register for a private demonstration, visit: www.calypto.com/events.php.

**Pricing and Availability**

Available now, Calypto's PowerPro CG runs on PC platforms running Linux and is priced at $295,000 (U.S.) for a one-year, time-based license. Existing PowerPro CG customers will be upgraded to the new version at no charge. SLEC RTL is available now and is priced at

$175,000 (U.S.) for a one-year, time-based license. Synthesis solutions are available directly from their manufacturers.

**About Calypto**

Founded in 2002, Calypto® Design Systems, Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class power optimization and functional verification software, based on its patented sequential analysis technology. Calypto, whose customers include Fortune 500 companies worldwide**,** is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor program, Si2 and is an active participant in the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America. Corporate headquarters is located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. More information can be found at: www.calypto.com.

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