Another Scary EDA Movie: DATE 2005

By Julien Happich, Associate Editor EPN

Every year, new thematics seem to emerge in the Electronic Design Automation industry, bringing with them a new set of scaremongers. Of course, many start-up companies invent just the niche solutions that will save IC designers, allegedly. The driving fear factors are not new; merely the ongoing race for smaller geometries with the obedience to Moore's law and some pressurised time-to-market windows. These were again the ingredients of DATE 2005, set in Munich last February, with terrible suspense building up on these uncanny PowerPoint presentation brick walls.

⇨ Embedded system level

SpiraTech and Novas Software have entered an OEM agreement whereby SpiraTech's Cohesive technology will supply transaction capture and generation technology for Novas' new nESL system debug product. Novas will offer SpiraTech's technology within its nESL product to automatically extract transaction information that inherently exists within system and hardware design and verification environments. Transactions will then be displayed both graphically and textually within the Novas nESL environment for debug and analysis. This visualisation can be performed dynamically during simulation using any leading HDL or SystemC simulator, or as a post- simulation function. At the transaction level, the combined tools will enable designers to analyse cause-and-effect behaviours of ESL or RTL designs for a wide variety of standard protocols, without the costly effort of creating their own transaction extractors.

Calypto Design System targets both RTL and system-level design and verification needs, planning to release in the second quarter of 2005 a solution for bridging the gap between ESL design and IC implementation at the register transfer level. This in turn would support faster verification times and design at a higher level of sequential abstraction. This technology will support a System-to-RTL continuum which, says the company, will allow users to navigate between various levels of abstraction in order to make system-level or micro-architectural changes to a design, quickly verify them, and then retarget the design towards an RTL implementation flow.