InsideChips.Ventures™

Tracking Fabless, IP & Design-House Startups

Volume 6, Number 7 July 2005

Business Microscope

3-D Chip Trends … For more than 30 years, chipmakers have been riding the Moore's Law speed and performance wave. Without fail, they have been able to rely on reductions in transistor size used in ICs to achieve predicted increases in speed and performance. Moore's Law, which states that chip performance doubles approximately every two years, held true because the RC delay has been negligible in comparison with signal propagation delay. For submicron technology, however, RC delay becomes a dominant factor. As the industry moves to submicron feature sizes, shrinking two-dimensional chips will become problematic.

One emerging solution is 3-D integration. The technology is not new but it is becoming increasingly important as researchers look for solutions beyond the perceived limits of today's two-dimensional devices.

InsideChips' Steve Szirom co-chaired the 3-D Architectures for Semiconductor Integration and Packaging Conference in Tempe, Ariz., held June 13-15. Organized by RTI International, the yearly conference explores market and technology opportunities in the 3-D space.

Universities, institutes/consortia, IDMs and a handful of startups are conducting 3-D research around the world. Table 1 (page 2) highlights the notable players. DARPA funds most of the university programs in the U.S.

Initial 3-D efforts involved package stacking or chip stacking in a single package with wire bond interconnects. Amkor is a good illustration of this approach. Begun in 1998, the technology was primarily used for memory stacks.

One of the early pioneers of 3-D, Irvine Sensors, developed stacked chips in which the connections are made over the edge of the die. One limitation, however, is that all die must be the same size. If a die shrink is implemented, the process requires considerable retooling.

Ziptronix uses a patented ZiROC and ZiCON bonding process

in this issue:

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that enables analog, memory and logic die —designed and produced in their optimum technologies — to be integrated as true chip-scale SOCs. This approach eliminates future scaling issues, and designers no longer need to compromise embedded memory or analog circuit functions.

(See our profile of Ziptronix in the Aug. 2003 issue of *InsideChips.Ventures*.)

Tezzaron Semiconductor (formerly Tachyon Semiconductor), which started out as design house, has moved into the 3-D arena and is developing its FaStack wafer-stacking technology. We believe the firm uses its own proprietary IP, licensed stacking technology and wafer-bonding technology co-developed with IME. Tezzaron's 3-D wafer-stacking technique is best suited for memory (DRAM, PCRAM, FeRAM, and MRAM) and FPGAs.

Continued on page 20

Table 1 -- Companies and organizations in the 3-D semiconductor space

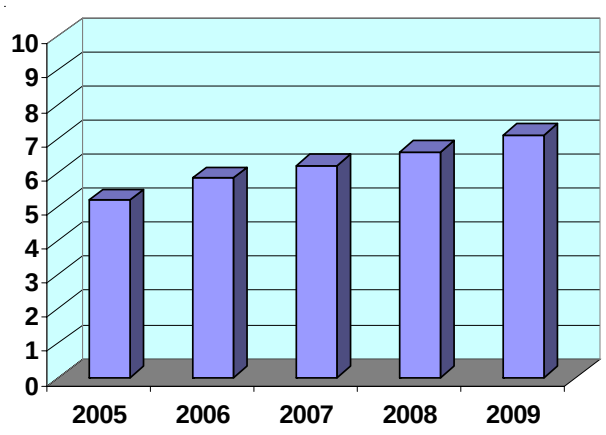
Institutes/Consortia	
ASET (1999-2001)	Japan
Fraunhofer	Germany
IMEC	Belgium
RTI	U.S.

Universities	
Albany Nanocenter	U.S.
Arkansas	U.S.
Delft	Netherlands
Lincoln Labs	U.S.
MIT	U.S.
RPI	U.S.
Tohoku Univ.	Japan

IDMs	
IBM	U.S.
Amkor	U.S.
Fujitsu	Japan
Infineon	Germany
Intel	U.S.
Micron	U.S.
Toshiba	Japan

Startups	
Contour Semiconductor	U.S.
Matrix Semiconductor	U.S.
Irvine Sensors	U.S.
Tezzaron Semiconductor	U.S.
Vertical Circuits	U.S.
Ziptronix	U.S.
ZyCube	Japan

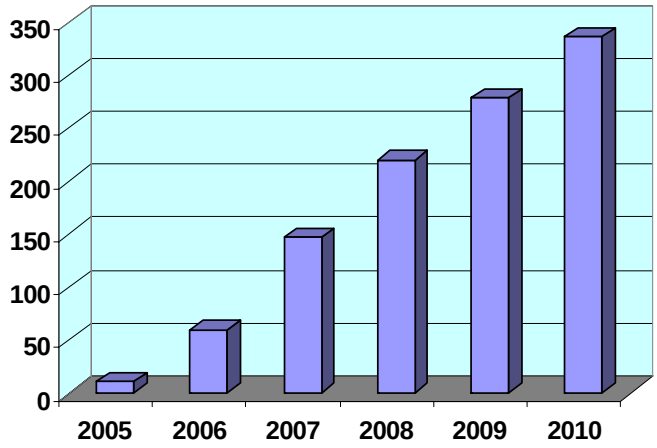
Worldwide High-Density NOR Flash Memory Revenue ($ Billions)



Source: iSuppli

Figure 1

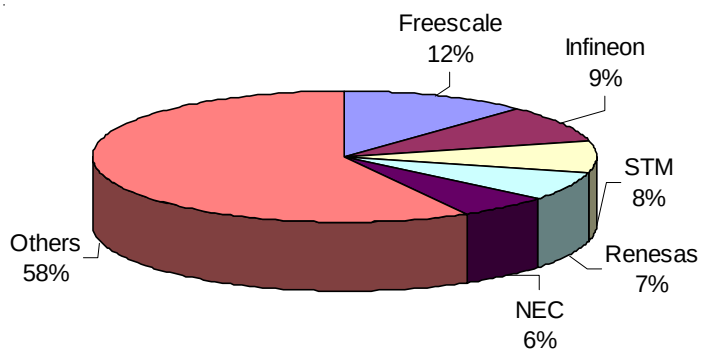
Worldwide Digital Audio Chip Sales ($ Millions)



Source: In-Stat

Figure 2

2004 Automotive Semiconductor Vendor Market Shares



Source: Strategy Analytics

Figure 3

Bits and Bytes

Cree to Close Silicon Microwave Business

Cree has revealed plans to close the silicon RF and microwave semiconductor business of its wholly owned subsidiary, Cree Microwave, located in Sunnyvale, Calif. This business manufactures silicon-based laterally diffused metal oxide semiconductor (LDMOS) and bipolar products.

Cree said it closed the business to focus on wide-bandgap RF and microwave products based on its silicon carbide (SiC) and gallium nitride (GaN) technology. The company also considered the financial outlook for the silicon RF and microwave semiconductor operations. For the nine months ended March 27, 2005, Cree incurred net operating pre-tax losses of $9.2 million related to this segment of its business.

Cree Microwave will accept last time buy orders for its silicon LDMOS products through June 2005, and plans to wind down the operations of this business by December 2005. The company estimates that it will incur a total of approximately $13 million to $15 million in pre-tax expenses to close the Sunnyvale facility.

The silicon RF business operated at the Sunnyvale facility has been referred to as the company's Cree Microwave segment for financial reporting purposes. Although this segment will no longer be used for financial reporting purposes, Cree's wide-bandgap RF and microwave products based on SiC and GaN technology will continue to be marketed under the Cree Microwave brand.

STMicroelectronics Sheds More Light on European Restructuring

STMicroelectronics has specified the restructuring efforts the company announced on May 16. The company presented principles of the initiatives, which will bring the cumulative reduction of its workforce in Europe — out of a total of 3,000 outside Asia — to 2,300 jobs by mid-2006, including the non-renewal of some temporary positions.

The following are some of the company plans to reorganize its European activities:

- Convert 6-inch production tools to 8 inches, in pursuit of the program already undertaken;
- Optimize its EWS activities (wafer test) on a global scale;
- Harmonize its support functions, reduce its costs and rationalize its activities (outside of manufacturing); and
- Disengage from certain activities.

STMicroelectronics said it will attempt to minimize the social impact of this reorganization by putting in place, whenever possible, measures that favor voluntary redundancy (early retirement measures, job creation schemes, individual projects, transition to part-time work).

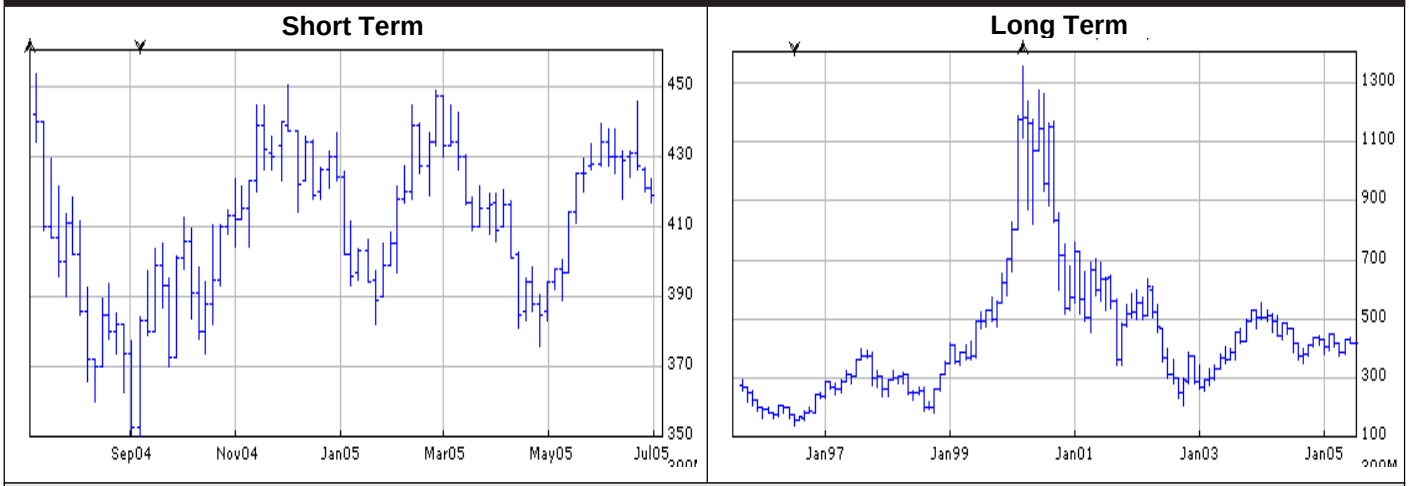
Lattice Places Two Top Execs on Leave

Lattice Semiconductor has placed CEO Cyrus Tsui and Rodney Sloss, VP of finance, on paid leave of absence pending completion of an independent examination being undertaken by the company's audit committee. Lattice named Stephen Skaggs acting CEO and Patrick Jones acting chairman of the board.

The audit committee is examining issues primarily associated with executive compensation and several related items pertaining to the company's internal controls. Lattice said it is not aware of any required adjustments to its historical financial results in connection with these matters. The company has furnished information regarding the matters under examination to the Securities and Exchange Commission, which is conducting an

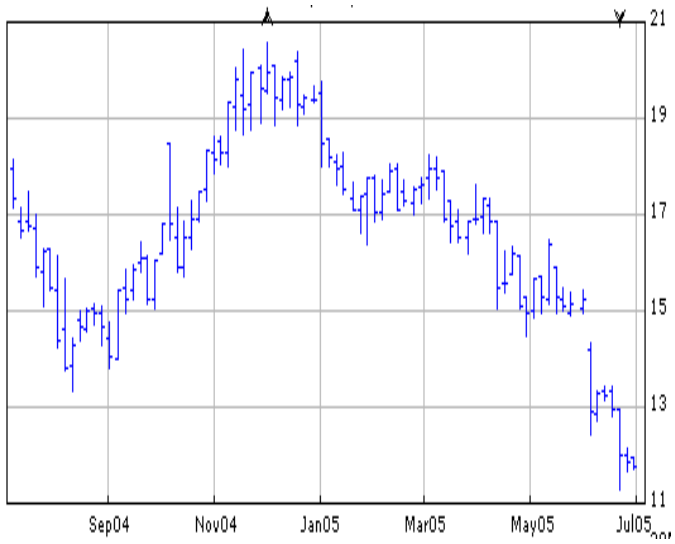
Continued on page 21

Semiconductor Stock Index

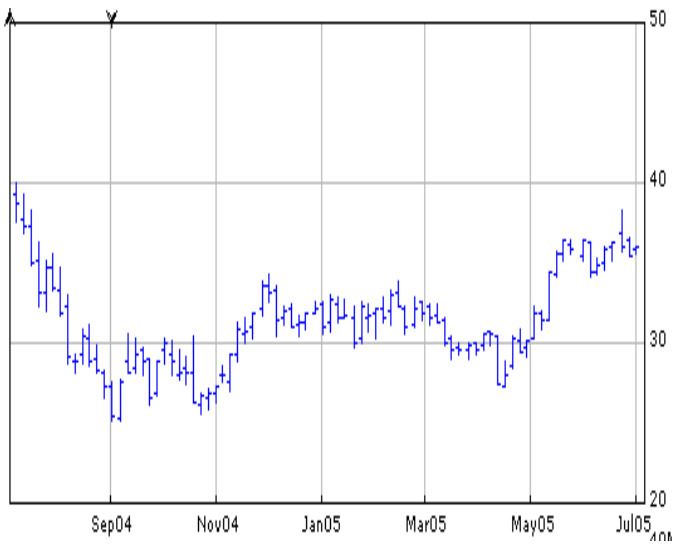


Stock Market Scan

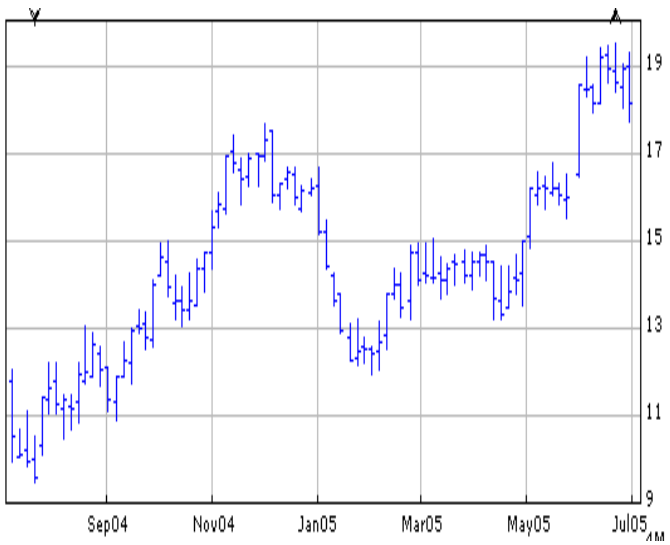
AMD



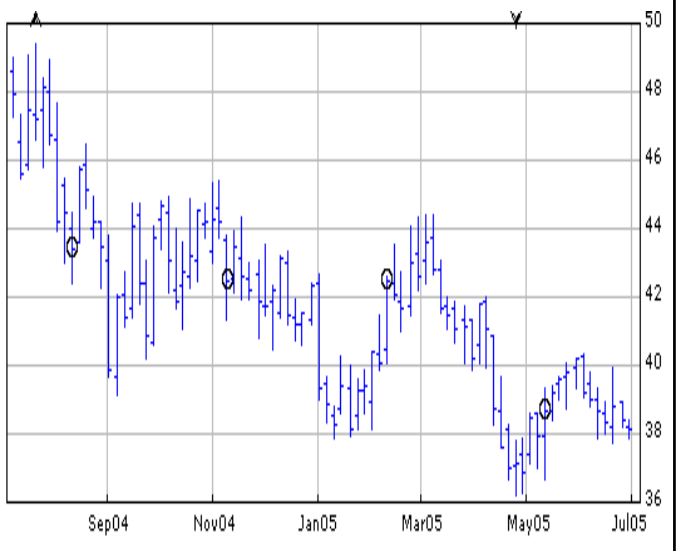
ATI Technologies



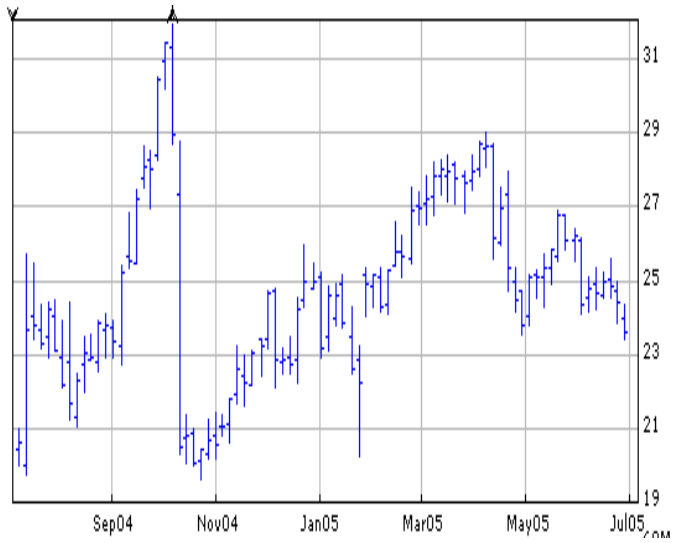
Broadcom



Genesis Microchip



Maxim Integrated Products



Sandisk

Finance: News, Funding and Acquisitions

Infineon Sells Wearable Electronics in Management Buyout

Within the framework of a management buyout (MBO), Infineon Technologies has turned over its activities in the area of wearable electronics to the company Interactive Wear of Wessling, Germany. Infineon, which had conducted research on the integration of electronic functions into textiles and developed this technology to the point that it is ready for the market, nevertheless discontinued these activities as part of its strategic restructuring and concentration on its core business.

As part of this MBO, which has now been completed, the rights to IP now belong to Interactive Wear, along with developmental hardware and software and the existing customer base, as well as the parts inventory and the finished wearable electronics products.

The companies did not disclose financial details of the transaction.

Infineon's former head of engineering for wearable electronics and current CTO at Interactive Wear, Markus Strecker, is participating in the MBO. Strecker, a sensor technology specialist, played a substantial role in the efforts that turned research results into marketable products. Former partner companies, consultants and industry insiders are supporting the MBO.

Andreas Roepert will assume the role of CEO, and Awa Garlinska will chair the supervisory board. All the people serving in Interactive Wear's management have either been in contact with Infineon (or Siemens, before it spun off Infineon) for many years or have served as executives in that company.

Stefan Jung, the former head of Infineon's activities in this field, has been appointed to Interactive Wear's supervisory board, and the company will also employ additional members of Infineon's technical team.

Contacts:
Andreas Roepert, Interactive Wear CEO; Tel: 08153-2819-45; www.interactive-wear.com
Dominik Asam, Infineon corporate VP for strategy, investor relations and mergers & acquisitions; Tel: 49 89 234 0; www.infineon.com.

Rudolph Technologies, August Technology to Merge

Rudolph Technologies, a provider of process control equipment for thin film measurement and macro defect inspection, is acquiring the much-sought-after August Technology, a supplier of inspection and defect analysis solutions for the microelectronic industries. The companies expect the deal to close in Q4 2005.

Each August shareholder will receive either $10.50 per share in cash or $10.50 per share in Rudolph stock, reflecting an aggregate consideration of approximately $193 million. The agreement requires that the total consideration for the transaction will include a minimum of $37.2 million and a maximum of $60 million of cash subject to shareholder election.

The combined company, which will be known as Rudolph Technologies, will employ approximately 600 people. The combined companies' 2004 revenues are approximately $160 million.

Rudolph's Paul McLaughlin and Steven Roth will continue to serve as chairman/CEO and CFO, respectively. August CEO Jeff O'Dell will join Rudolph's board of directors, and August CFO Stan Piekos will become Rudolph's chief corporate development officer. The company's board will increase to 12 people, including eight members from Rudolph, three members from August, and one additional board member to be jointly appointed.

August's merger with Rudolph comes after months of considering the pros and cons of several suitors that have been vying for the equipment company. August signed a merger agreement with metrology company Nanometrics in January, which was followed by an unsolicited takeover attempt by Rudolph one week later and an offer by KLA-Tencor in February to purchase August for $11.50 per share.

August paid a termination fee of $8.3 million, plus expenses, to Nanometrics.

August said it was concerned that an August/KLA-Tencor transaction would involve significant antitrust risk, including a lengthy investigation by the Department of Justice.

The new Rudolph will be headquartered in Flanders, N.J., and maintain the inspection business in Bloomington, Minn., and the metrology business based in New Jersey.

Contacts:
Paul McLaughlin, Rudolph CEO; Tel: 973 691-1300; www.rudolphtech.com.
Jeff O'Dell, August CEO; Tel: 952 820-0080; www.augusttech.com.

Semtech Acquiring XEMICS

High-performance analog and mixed-signal semiconductor provider Semtech is buying XEMICS, a fabless developer of ultra-low-power analog, RF and digital ICs. Semtech International, Semtech's wholly owned Swiss subsidiary, is the business entity acquiring XEMICS, which will be known as the Wireless and Sensing Products business unit.

Semtech International will pay $43 million in cash to the shareholders of XEMICS and has agreed to pay up to an additional $16 million if certain performance milestones are met within a 12-month period ending April 30, 2006.

XEMICS is an R&D-intensive company with 77 employees, of which 56 are actively engaged in the area of R&D. The company is privately held and based in Switzerland. XEMICS applies its low-power, low-voltage design expertise across its core technologies: sensor interfacing/data acquisition, 8-bit RISC microcontrollers, RF transceivers and audio codecs.

XEMICS was established in 1997 as a spin-off of the Swiss Center for Electronics and Microtechnology (CSEM). CSEM, which is funded by both government and industry sources, carries out applied research and product development. XEMICS works closely with CSEM on commercializing new technologies and expects to continue to do so after the acquisition.

In CY 2004, XEMICS generated net sales of about $23 million, mostly from custom and standard IC products for battery-powered applications, remote metering, embedded systems and medical devices. Gross margin during this period was 48%.

Contacts:
Jason Carlson, Semtech president and CEO; Tel: 805 498-2111; www.semtech.com.
Alain Dantec, XEMICS CEO; Tel: +41 32 729 4000; www.xemics.com.

JDS Uniphase Acquires Photonic Power Systems

JDS Uniphase has acquired Photonic Power Systems, a fabless semiconductor company providing GaAs and InP-based solutions for delivering electrical power over fiber for electronic applications. All eight of Photonic Power Systems' employees, currently located in Cupertino, Calif., will transition to JDSU's corporate offices in San Jose. The group will form the nucleus of JDSU's Photonic Power Business Unit, led by Jan-Gustav Werthen. The companies did not disclose financial details of the transaction.

Photonic power is an inventive power delivery system whereby light from a laser source illuminates a highly efficient photovoltaic power converter to produce electrical power. It is a novel approach to power delivery in specialty applications.

Photonic power replaces copper and batteries for remote sensors, coaxial cable in wireless applications, and oil or gas-filled measurement transformers in high-voltage applications. It delivers isolated power that is immune to RF, EMI, high voltage and lightning. Photonic Power Systems has deployed more than 10,000 units to date, serving more than 50 customers.

Contacts:
David Gudmundson, JDSU VP of corporate development; Tel: 408 546-5000; www.jdsu.com.
Jan-Gustav Werthen, Photonic Power Systems founder and CEO; Tel: 408 725-7597; www.photonicpower.com.

IDT, Integrated Circuit Systems to Merge

Integrated Device Technology (IDT) and Integrated Circuit Systems (ICS) have signed a definitive agreement to combine the two companies in a strategic merger. Under the terms of the merger agreement, which has been unanimously approved by the boards of directors of both companies, ICS stockholders will receive 1.3 shares of IDT common stock and $7.25 of cash for each share of ICS stock. Based on closing prices as of June 15, 2005, this total consideration values ICS at approximately $1.7 billion, or $23.54 per share.

Greg Lang, IDT president and CEO, will serve as president and CEO of the combined company, and Hock Tan, ICS president and CEO, will assume the role of chairman of the board. Tan will also have an executive role in the integration of ICS with IDT. The board of directors of the combined company will have nine members, with IDT designating five directors, including Lang, and ICS designating four directors, including Tan.

For the twelve months ending March 31, 2005, the combined company had revenues of approximately $645 million and generated $86 million in operating cash flow. The combined company will retain the IDT name and its stock will continue to trade on the Nasdaq national market under the ticker symbol "IDTI." The merged company will be headquartered in San Jose, Calif.

Based on the most recent capitalization, current IDT stockholders will own approximately 54% and current ICS stockholders will own approximately 46% of the combined company. The companies expect the transaction to be completed in fall 2005.

Contacts:
Greg Lang, IDT president and CEO; Tel: 408 727-6116; www.idt.com.
Hock Tan, ICS president and CEO; Tel: 610 630-5300; www.icst.com.

Aegis Spins Off Redshift Systems

Aegis Semiconductor, a supplier of wavelength monitoring and control solutions, has spun off RedShift Systems, which will enable low-cost and high-performance thermal imaging solutions for mass markets. Aegis has provided seed financing to RedShift.

RedShift's core technology enables manufacturers to include high-quality thermal imaging capability in a wide variety of products, but at one-tenth the cost of existing solutions. RedShift expects this price performance will not only position the company to disrupt an established $2 billion market for military, firefighting and industrial thermal imaging, but also open up new markets for thermal imaging in price-sensitive markets such as automotive safety, law enforcement, and video surveillance.

RedShift can offer such significant cost savings over current infrared vision technology in part because its platform can transform virtually any standard commercial camera into a thermal camera. This ability enables manufacturers to build on top of the hundreds of millions of commodity CMOS/CCD sensors that are produced annually and to take advantage of the large, ongoing industry investments to improve these sensors' performance and reduce their cost.

Originally developed at Princeton University and further commercialized by Aegis, RedShift's core technology is mature — the Aegis technology from which it was born is now operating in major telecommunications platforms — and may be manufactured using standard processes in volume foundries.

Matthias Wagner, co-founder of Aegis Semiconductor, has left Aegis to lead RedShift Systems as its CEO. Wagner had served as CEO of Aegis until February, when he handed off that post to Donald Bossi, who previously held a number of senior management positions at JDS Uniphase.

Aegis co-founder and CTO Eugene Ma has also joined RedShift, where he will assume the same position.

(See our profile of Aegis Semiconductor in the Dec. 2004 issue of *InsideChips.Ventures*.)

Contact:
Matthias Wagner, RedShift CEO; Tel: 781 672-2660; www.redshiftsystems.com.

Tehuti Networks Secures $4.2 Million in Series A Funding

Tehuti Networks, a semiconductor company providing TCP/IP acceleration processing for enterprise IT environments, has completed a $4.2 million Series A financing round. New investor Alice Ventures led the round, which included previous investors Alice Lab and ProSeed Venture Capital Fund. In addition, the Chief Scientist of the Government of Israel contributed funds.

Tehuti develops SOCs for accelerating TCP/IP processing. The company is developing network traffic accelerator (NTA) chips that increase system performance up to five times, relieving the bottleneck that occurs as the speed in

Ethernet networks increases faster than computer processor speeds. With no cost-adder over conventional, lower-performance implementations, Tehuti's low-power chips are transparent to the operating system and move specifically selected TCP/IP processing functions from software onto hardware, redistributing functions to remove TCP bottlenecks and reducing latency.

(See our profile of Tehuti in the Jan. 2005 issue of *InsideChips.Ventures*.)

Contact:
Arie Brish, CEO; Tel: 972-9-951-4180; www.tehutinetworks.com.

Agere Sells RF LDMOS Transistor Portfolio to Peak Devices

RF Transistor manufacturer Peak Devices has acquired Agere Systems' RF Power LDMOS portfolio, including the production wafers, die, packages, lids and select specialized assembly equipment for the manufacture and support of transistors that produce more than 10 watts of RF power.

LDMOS (laterally diffused metal oxide semiconductor) is a semiconductor technology that produces exceptional RF performance at frequencies up to 3 GHz, relative to traditional silicon device technologies such as bipolar and VDMOS (vertically diffused metal oxide semiconductor). The LDMOS semiconductor has the added benefit of low-cost packaging, as it does not require an insulator between the semiconductor and the package in which it is encapsulated.

The acquisition marks the completion Agere's plan to divest its RF power-related assets. In April, Ciclon Semiconductor Device, a developer of high-frequency LDMOS products, acquired the RF LDMOS product line of Agere Systems.

Both acquisitions are part of Agere's plan to focus resources on core technologies.

Contacts:
William McCalpin, Peak Devices CEO; Tel: 720 406-1221; www.peakdevices.com
Carlos Garcia, Agere VP of marketing for Telecom division; Tel: 610 712-4323; www.agere.com.

Tharas Secures $5.5 Million in Funding

EDA startup Tharas Systems has raised $5.5 million in new venture capital funding. El Dorado Ventures led the financing round, which included current investors NeoCarta Ventures; Alliance Venture Management; Andy Bechtolsheim, co-founder of Sun Microsystems; and Tharas board member Prabhu Goel.

Founded in 1998, Tharas develops design verification appliances that lead to a significant shortening of the overall verification cycle of complex ICs and electronic/embedded systems. The company's recently introduced Hammer S-Class and M-Class product families incorporate a patented, multi-core, custom-processor hardware-assisted engine developed by Tharas for use in Verilog- and VHDL-based SOC and embedded system verification.

Contact:
Rahm Shastry, president and CEO; Tel: 408 855-3200; www.tharas.com.

Intel Establishes $200 Million China Venture Fund

Intel has established a $200 million venture capital fund to invest in Chinese technology companies developing innovative hardware, software and services. Intel expects the Intel Capital China Technology Fund to stimulate local technological innovation and accelerate technology adoption locally.

The Intel Capital China Technology Fund will be used to invest in companies that complement Intel's technology initiatives and to further build out the Internet infrastructure in China. The fund will also provide local businesses with capital to help nurture important technologies and products developed in China. Examples of initial focus areas include cellular communications, broadband applications for consumers, and semiconductor design.

Intel Capital, which has investment managers based in Hong Kong, Shanghai and Beijing, made its first strategic investment in China in 1998 and has since invested in close to 50 Chinese companies across nine cities in mainland China and Hong Kong. Eleven of these companies have gone public or have been acquired, including AsiaInfo Holdings, a telecom software supplier; Chinacast Communications Holding Ltd., a total solution service provider for remote education; Sohu.com, an Internet portal; Techfaith Holdings Ltd., an independent cell phone design house; and UTStarcom, a telecom equipment manufacturer.

Examples of current Intel Capital investments in China include BCD Semiconductor Manufacturing, an analog power IC design and manufacturing company; Comlent Holdings, an RF chip maker; HiSoft Technology International, a software outsourcing company; Maipu Holdings, a router and data communications company; and Pollex Mobile Holdings, a cellular phone software applications provider.

Contact:
Arvind Sodhani, Intel Capital president; Tel: 408 765-8080; www.intel.com/capital.

Clear Shape Technologies Closes Series B Financing Round

Clear Shape Technologies, a semiconductor design for manufacturing (DFM) software and technologies startup, has raised more than $5 million in its second round of venture financing, bringing total funding to more than $10 million. Intel Capital led the most recent round, which also included KT Venture Group (the investment partner of KLA-Tencor). Early in 2004, U.S. Venture Partners led the Series A financing with participation from Telos Ventures and AsiaTech Management.

Founded in 2003 by a veteran team of experts in the semiconductor manufacturing and EDA industries, Clear Shape Technologies develops design for manufacturing (DFM) software and technologies that detect potentially catastrophic manufacturing failures during design, improve yield, and enable designers to control, manage and optimize the impact of systematic variation on chip performance, signal integrity, and leakage power while protecting manufacturing IP.

Contact:
Atul Sharan, Clear Shape president and CEO; 408 833-7130; www.clearshape.com.

MOSAID Withdraws Offer to Acquire TriCN

After signing a non-binding letter of intent to acquire the assets of TriCN for $3.1 million in May, MOSAID Technologies has decided that, as a result of due diligence, it will not proceed with the acquisition.

TriCN filed for protection under Chapter 11 of the United States Bankruptcy Code on Dec. 30, 2004.

Founded in 1997, TriCN is based in San Francisco, Calif., and is a developer of high-performance semiconductor interface IP products.

Contact:
Peter Gillingham, VP and GM of IP Division; Tel: 613 599-9539; www.mosaid.com.

Flextronics Selling Network Services and Semi Groups

Flextronics has signed separate agreements for the sale of Flextronics Network Services (FNS) and Flextronics Semiconductor.

As previously announced in May, FNS will merge with Telavie, a company wholly owned by Altor 2003 Fund, a Nordic private equity firm. Under the terms of the agreement, Flextronics will receive an upfront cash payment, deferred and contingent payments, and will also retain a 30% ownership stake in the merged company. FNS, a global network services provider, has annual revenues of approximately $770 million. Telavie, a Scandinavian network services group, has annual revenues of approximately $230 million. The merged company will employ nearly 10,000 people throughout 18 countries with total revenues of approximately $ 1 billion.

In a separate agreement, Flextronics will sell its semiconductor division for cash to AMIS Holdings, parent company of AMI Semiconductor, for $135 million in cash. Flextronics Semiconductor specializes in custom mixed-signal products, imaging sensors and digital ASICs, including FPGA conversion products. The proposed sale, structured as an asset purchase agreement, includes these three divisions, which collectively employ approximately 200 people in the United States, the Netherlands and Israel.

As a result of the two transactions, Flextronics will receive an aggregate upfront cash payment in excess of $550 million plus additional deferred and contingent payments and a 30% ownership stake in the merged network services company. Flextronics expects both transactions to close before the end of the Sept. 30 fiscal quarter.

Flextronics intends to concentrate its efforts and resources on the core EMS business, which includes design, vertically integrated manufacturing services and logistics.

Contacts:
Michael Marks, Flextronics CEO; Tel: 408 576-7000; www.flextronics.com.
Harald Mix, Altor CEO; Tel: +46 8 678 91 00; www.altor.com.
Christine King, AMIS president and CEO; Tel: 208 233-4690; www.amis.com.

ChipMOS Taiwan and Chantek Agree to Merge

ChipMOS Technologies and Chantek Electronic, a subsidiary 68% owned by ChipMOS, have agreed to merge in a stock-for stock transaction.

Under the terms of the merger agreement, Chantek will be de-listed from the Taiwan GreTai market and merged into ChipMOS Taiwan, with ChipMOS Taiwan as the surviving entity. Chantek stock will be exchangeable for ChipMOS Taiwan stock at the ratio of 3.6 to 1. Shareholders of Chantek may elect to receive cash payment of approximately $0.19 per Chantek share in lieu of shares of ChipMOS Taiwan. ChipMOS expects to close the merger on Nov. 1, 2005.

ChipMOS is an independent provider of semiconductor testing and assembly services primarily to customers in Taiwan, Japan, and the U.S. The company has advanced facilities in Hsinchu and Southern Taiwan Science Parks in Taiwan and in Shanghai, China.

Contact:
S.J. Cheng, ChipMOS CEO; Tel: 886-3-577-0055; www.chipmos.com.tw.

Winbond Acquires NexFlash Technology

Winbond Electronics has acquired 46% in stock shares of NexFlash Technology via Winbond's wholly owned overseas subsidiary, Winbond International. Winbond first acquired 54% of Nexflash stock in Jan. 2001. With this acquisition of the remaining 46% of Nexflash stock, Winbond will now own 100% stock shares of NexFlash.

NexFlash Technology primarily focuses on flash memory technology and related products. It owns a variety of patents for high-density data flash and code flash products. NexFlash has a full spectrum of serial flash products ranging from 2 MB to 32 MB capacities. These products are all manufactured by Winbond's 0.18-micron WinStack process technology in Winbond's 8-inch fab.

With serial flash memory's low cost advantage, the technology trend for low-density flash has gradually moved from parallel flash memory toward serial flash memory. The acquisition enables Winbond to provide total solutions for its customers.

Winbond also named Arthur Y. C. Chiao as chairman and CEO of the company, C.C. Chang as vice chairman and deputy CEO, and I.S. Hsu president and COO (effective Aug. 1).

Chang, who took over the presidency in Jan. 1999, led Winbond into the specialty DRAM business. As vice chairman and deputy CEO, he will continue to assist in the management of the company's operations, and he will also be in charge of technology development, knowledge/MIS management and financial management.

Hsu has held various positions at Winbond, including the director of the Personal Computer Business division, the sales AVP and VP, and the VP of the logic business group.

Contact:
C.C. Chang, vice chairman and deputy CEO; Tel: 886-3-5770066; www.winbond.com.

HelloSoft Completes $16 Million Series B Financing Round

HelloSoft, a supplier of signal-processing technology and software-defined radio (SDR) solutions, has closed an oversubscribed $16 million series B financing. Boston-based TD Capital Ventures led the round, which included new investors Mitsui & Company Venture Partners and Entrepia Ventures, and current investors Venrock Associates, Sofinnova

Ventures and Jump Startup.

Headquartered in San Jose, Calif., HelloSoft is a pioneer in VOIP solutions and maintains a WLAN and cellular IP portfolio. The company's solutions enable cost-efficient mass deployment of multi-mode mobile communications devices for the converged market place. The company also has an R&D facility staffed with more than 100 DSP engineers in Hyderabad, India.

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picoChip Secures $20.5 Million in Third-Round Funding

Wireless silicon solutions provider picoChip has secured $20.5 million in its third round of funding. New investor Scottish Equity Partners led the round, which also included Rothschild and Intel Capital, along with previous investors Pond Venture Partners and Atlas Venture. The round brings total company funding to $41.5 million.

Founded in 2000, Bath, England-based picoChip developed a scalable, multi-processor baseband IC that combines the computational density of a dedicated ASIC with the programmability of a traditional high-end DSP. Equipment based on picoChip technology will enable telecom operators to remotely re-configure and upgrade their equipment without the high costs of replacing obsolete hardware.

(See our profile of picoChip in the Aug. 2002 issue of InsideChips.Ventures.)

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Therma-Wave Sells Integrated Metrology Module to TEL

Therma-Wave, a developer of process control metrology systems used in semiconductor manufacturing, has entered into an agreement to sell its Compact Critical Dimension-integrated (CCD-i) product to Tokyo Electron Limited (TEL) in a cash transaction valued at approximately $9.95 million.

The transaction includes the transfer of certain tangible assets, IP and personnel related to the applications, support and manufacturing of the CCD-i product line to TEL. Therma-Wave supplied CCD-i systems to TEL through the end of the first quarter of fiscal year 2006, ended July 1, 2005. As a result of this transaction, Therma-Wave will remove $5.65 million in previously received orders from TEL for CCD-i products and services from the company's backlog.

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Hikaru Ito, TEL VP and GM of Clean Track Business Unit; Tel: 03-5561-7000; www.tel.com

SCP Sells Single-Wafer Clean Technology to Applied Materials

SCP Global Technologies is selling its single-wafer cleaning technology and related IP for an undisclosed amount of money to Applied Materials. The acquisition includes SCP's single-wafer HF-last immersion technology and Marangoni clean/dry IP. Marangoni clean/dry technology is an industry standard for 65-nm-and below wet clean processing.

The transaction is SCP's first step in establishing its new strategy as a services company to the wafer wet cleaning equipment industry. The initial focus will be on the extensive installed base of tools SCP has sold to its customers globally. Services will include upgrades to enhance performance, spare parts, repairs and onsite maintenance contracts.

SCP has an extensive IP portfolio it uses in its own equipment, as well as licenses to other manufacturers of surface cleaning products.

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John T.C. Lee, Applied Materials GM of Cleans Product Group; Tel: 408 727-5555; www.appliedmaterials.com.

LanOptics Increases Equity Interest in EZchip Technologies

Network processor provider LanOptics has entered into an exchange agreement under which it will increase its ownership interest in the outstanding share capital of its EZchip Technologies subsidiary from 53.4% to 58.7%. LanOptics' business consists exclusively of the business of EZchip, a company that is engaged in the development of high-performance network processors.

LanOptics will acquire 3,611,243 EZchip shares held by certain investors, in exchange for the issuance of 1,006,486 LanOptics shares. The exchange ratio was determined based solely on the parties' respective holdings in EZchip. As a result of the exchange ratio mechanism, the economic interest of each LanOptics shareholder should remain unchanged despite the resulting dilution in each shareholder's percentage of ownership.

This transaction represents another step in LanOptics' long-term plan to acquire 100% ownership of EZchip, authorized by LanOptics' shareholders in April 2003. LanOptics will seek to further increase its holdings in EZchip by pursuing similar exchange agreements with other EZchip shareholders.

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Innovative Silicon Secures $16 Million in Series B Funding

Innovative Silicon, the developer of Z-RAM zero-capacitor DRAM embedded memory technology, has closed its $16-million series B round of investment. New investor Austin Ventures led the round, which included existing investors Index Ventures, Auriga Partners and SOI specialist Soitec. Innovative will use the financing to expand sales and marketing initiatives for its ultra-high-density memory technology.

Founded in 2002, Innovative Silicon has developed a new kind of memory technology that can achieve five times the density of embedded SRAM and twice the density of embedded DRAM while using a standard SOI logic process. Z-RAM harnesses the floating body effect of SOI semiconductors to store the charge in the body of the transistor and eliminate the capacitor.

(See our profile of Innovative Silicon in the June 2005 issue of *InsideChips.Ventures*.)

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Analyzing the Analysts

NAND Grew Faster than Any Other Semiconductor Market in 2004

According to a new report by Semico Research, NAND was the fastest-growing market in the semiconductor arena in 2004. Revenues jumped a whopping 80% to $7.2 billion. Even so, NAND continued to trail NOR, which ended 2004 at $9.1 billion. These two flash technologies lead the nonvolatile market, combining to account for 91% of all nonvolatile memory revenues. ROM, EPROM, and EEPROM revenues each accounted for less than $1 billion in revenues.

Samsung led the pack in total nonvolatile as well as in NAND, owing to its dominant 54% share of NAND revenues. The company was able to take $2 billion of the $3.2 billion growth in 2004's NAND market. Spansion displaced Intel for leadership in NOR, despite Spansion's eroding share toward the end of the year. Macronix, Oki, and Atmel took the top spots in ROM, EPROM, and EEPROM, respectively.

The size of the NAND market came as something of a surprise to Semico, as WSTS reported lower revenues for the same year of only $6.5 billion. Semico verified its findings with market participants to ascertain the accuracy of the survey's findings, and the larger number was confirmed.

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802.15.4 Market Could Grow 200% by 2009

The market for 802.15.4, a wireless personal area networking (PAN) technology, and the ZigBee specification network layer, are poised for skyrocketing growth, reports In-Stat. On an aggressive basis, 802.15.4 nodes/chipsets could grow by a compound annual growth rate (CAGR) of 200% from 2004 to 2009, with annual shipments surpassing 150 million units in 2009.

In December 2004, the ZigBee Alliance completed a major milestone -- final signoff of the ZigBee 1.0 specification. Even considering proprietary competition, the benefits promised by 802.15.4 and ZigBee standardization still hold true. Although standardization takes longer, a major advantage of 802.15.4 and ZigBee is that they provide OEMs with a menu of multiple silicon sources and ZigBee networking layer suppliers. Additional advantages include pricing competition and system vendor partnering opportunities.

Commercial building control is expected to capture the lion's share of the 802.15.4 market, in terms of node/chipset volumes, but not design wins. InStat also expects that, together, system-in package (SiP) and system-on-chip (SOC) solutions will drive easier system/product development and lower the costs of adding this wireless capability to sensor networks.

The report, "802.15.4 SoC and SiP Surge as ZigBee Faces Residential Competition," is priced at $2,995.

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SEMI Reports 20 New Fabs to be Built in China by 2008

According to a new market research report from SEMI, new semiconductor equipment sales in mainland China reached $2.73 billion in 2004, used/refurbished equipment sales reached an estimated $180 million, fab materials sales totaled $391million, and the packaging materials market reached $781 million.

The report, entitled, "China Capital Equipment and Electronic Materials Market Outlook," points out that while China's semiconductor manufacturing is a relatively small share of the world total, 20 new fabs are expected to be built in China between 2005 and 2008, many of which will be equipped with used and refurbished equipment.

Furthermore, the number of silicon wafers consumed in China increased dramatically, while the first 300-mm fab began pilot production in 2004.

The report identifies semiconductor market trends and forecasts for the markets in China for equipment, fab materials, packaging materials and indirect materials. Some of the key findings include:

- Installed 200-mm and 300-mm wafer capacity at the end of 2004 was equivalent to 106 million square inches (MSI) per year.
- Many of the 150-mm (and smaller diameter) fabs have been equipped with used or refurbished equipment.
- Chinese companies have lobbied the government to invest in R&D for high-end tools.
- The local supply chain remains immature because of financial/capital considerations and current limitations with locally available skilled talent; some multinationals are cautious about working with local companies because of intellectual property concerns.
- China is home to more than 35 domestic, joint venture and multinational semiconductor manufacturers with wafer-fabrication plants.
- There are approximately 200 assembly and test companies, 20 multinational packaging materials suppliers, and 40 domestic manufacturers of equipment for the semiconductor and related microelectronic industries in China.

SEMI is selling the report for $3,000 (SEMI members/single user), and $4,000 (non-members/single user).

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Table 2 — Estimated silicon wafer consumption in China (annual wafer consumption)

Diameter	2003	2004	Percent Growth
100 mm or smaller	2,250,000	2,750,000	22%
125 mm	880,000	1,150,000	31%
150 mm	1,610,000	2,780,000	73%
200 mm	860,000	1,700,000	98%

Nethra Imaging

Founded by former MediaQ executives, Nethra Imaging is developing digital camera chips intended to take cameras embedded in phones to 3 megapixels. The company's objective is to provide imaging solutions for phones and other mobile devices that are as high quality as digital SLR cameras.

Two MediaQ alumni, Ramesh Singh and Murty Bhavana, co-founded Nethra with Ravi Bhatnagar in late 2003. Singh, who serves as president and CEO, was most recently VP of sales at NVIDIA. He joined NVIDIA through the acquisition of MediaQ, which he founded and where he served as president and CEO and VP of sales. Prior to founding MediaQ, Singh was the GM of the Home Products Division (3D graphics products) at S3, and he also held positions with Chips & Technologies and Rockwell Collins.

Bhavana, VP of marketing, was previously the director of marketing for MediaQ and director of marketing at NuCORE Technology. He has also worked as a consultant in the imaging industry, where his clients included early-stage companies, such as Pixim (image sensors) and Atsana (application processors).

Bhatnagar, senior VP of engineering, was senior VP of business development at NeoMagic. He came to NeoMagic through the acquisition of LinkUp Systems, which he founded and where he served as the president and CEO. Prior to LinkUp, Bhatnagar was the VP of engineering for the Personal Systems Division at Cirrus Logic and VP and GM of the New Products (microprocessor) and Systems Logic Divisions at Chips and Technologies.

Nethra, which means human eye in Sanskrit, closed its second round of funding in Nov. 2004, which brought the total funding raised so far to $10.5 million.

Today, CMOS image sensor vendors build the image processor into the sensor as a monolithic system. As camera phones advance to 2 and 3 megapixels, however, space constraints prevent the sensor from scaling up further, with the result that the quality of the image processing decreases.

Handset makers, therefore, are starting to request that the sensor guys remove the image processing from the sensor. One kind of emerging architecture, from companies such as Qualcomm, Texas Instruments, nVIDIA and ATI Semiconductor, involves integrating the image-processing functionality into their applications processor or applications/baseband processor.

Nethra is pursuing a different architecture, in which a discrete image processor is embedded into the module or sits on the main system board. The company's solution works with both CMOS and CCD sensors.

Although Nethra's solution adds an additional chip, a big advantage is that it eliminates the problem of software integration – which is significant, as the software integration challenge increases as functionality increases. Nethra's architecture has an on-board CPU, embedded flash, and optional integrated SDRAM. The company's products embed software needed to tune the picture quality and system control in the embedded flash, essentially limiting the OEMs' integration time to testing.

Nethra's target space is mid-market to high-end phones that have the ability to produce print-quality images. This rules out "give-away" phones, the basic phones subsidized by carriers and provided to customers; those phones will continue to employ the current integrated sensor/image-processing architecture, which is inexpensive, or the emerging architecture discussed above in which image-processing functionality is integrated into the applications or applications/baseband processor.

Nethra-enabled phones will be premium products that must provide print quality images and no-compromise image processing. The company's market begins with phones for which carriers charge a $50 or $100 premium, and goes all the way up to PDA-type phones.

Nethra's first product line is the NI-20x0 family of SOCs, which include an image-processing engine, 32 KB of SRAM, 64 KB of embedded flash memory, an embedded ARM7TDMI core and SDRAM (in some versions) in an 8-mm-square chip-scale package with 1.0- to 1.2-mm mounted thickness. System peripherals include pulse-width modulators, general-purpose input-output devices and serial peripheral interfaces.

The NI-2080 and NI-2090 products have 8 MB and 2 MB, respectively, of integrated SDRAM, and the NI-2070 supports external SDRAM. However, Nethra does not believe these three will be very high volume; the bread and butter for the company will be the NI-2060, which does not include any SDRAM support in the package.

High-end digital still camera features in the NI-2060 include:

- Auto white balance and auto exposure;
- Programmable lens shading compensation;
- Adaptive low-light performance; and
- Histogram and statistical engine.

The NI-2060, 2080 and 2090 are all pin-compatible, enabling handset OEMs or module vendors to design a single platform or module and drop in the three different parts for different price points.

Nethra also sells a bare-die version, the NI-2050, which primarily serves as a replacement for NI-2060 designs in which a thinner form factor is required.

To compensate for any problems associated with the optics, Nethra employs correction algorithms that are sufficiently flexible and programmable to support any kind of optics technology. In fact, an OEM that was originally planning to go to market with a CCD sensor can now consider the possibility of using a CMOS sensor. Nethra is not claiming it can make CMOS sensors look as good as CCDs, but it maintains that its advancements have helped to bridge the gap.

Nethra's potential customers are split between module vendors and handset OEMs. While "candy bar" phones typically integrate the image processor on the system board, flip phones typically have the camera embedded on the flip side and represent a module play.

Nethra is currently focused primarily on

the module developers, which tend to be on shorter design cycles. However, to get into certain key designs requires the company to get its chips onto the system board, and Nethra is working with OEMs and existing partners to stack its die inside a packaged part from the partner vendor.

Several other companies are also working on chipsets with a similar kind of discrete image processor architecture. SunPlus, WinBond and NEC, for example, supply just the image processor. MTekVision and Texas Instruments, as with Nethra, are developing image processor + CPU architectures. Nethra maintains that the amount of detail its image processor technology can pick up is far superior to these competitors.

Nethra's management team includes Phil Barnes as VP of sales. Barnes is a 25-year industry veteran with engineering, marketing and sales experience at large corporations such as LSI Logic, Cirrus Logic and Toshiba Electronics, as well as smaller organizations and startups such as Headland Technology and MediaQ.

Ping Wah Wong, VP and chief imaging scientist, previously managed a research team at Hewlett-Packard Laboratories that developed imaging algorithms and pipelines for HP products. At HP's Internet Imaging Organization, he managed a software team that built imaging servers for multiple Unix and Windows platforms.

Surin Chowdhury serves as director of operations. Prior to joining Nethra, Chowdhury served as director of engineering at Platys Communications. After Adaptec acquired Platys in 2001, he set up a physical design team at Adaptec's engineering subsidiary in Hyderabad, India. Chowdhury was also director of multimedia engineering operations at Sierra Semiconductor and operations manager at VLSI Technology, and has held engineering manager roles at National Semiconductor and AMI.

Srini Amble, director of software engineering, has worked for AT&T Bell Labs, Fujitsu and several startups.

Katz Hanazaki, director of business development, Japan, was previously senior manager of the handheld division at NVIDIA's Japan office. Prior to NVIDIA's acquisition of MediaQ, Hanazaki was GM at MediaQ's Tokyo office. He has also worked at Cirrus Logic and TI.

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Optichron

Optichron is a Fremont, Calif.-based startup pioneering a new approach to nonlinear signal processing for communications applications. Based on a proprietary architecture, the company's linearization IC is the silicon engine at the heart of a line of high-speed nonlinear signal-processing modules.

Roy Batruni, Tim Ryan and Ravi Ramachandran founded Optichron in Jan. 2003. Batruni, who serves as CEO, began his career at National Semiconductor, where he spent 15 years in the company's Telecom and Mass Storage groups. His last position there was director of the DSP Group. After National, he worked at startups ControlNet and Enable Semiconductor. Later, Batruni served as VP of engineering for Avio Digital, acquired by Centillium Communications. At Centillium, he held the same title and was responsible for the development of high-performance ADSL products.

Ryan, the company's director of systems engineering, previously co-founded Avio Digital in 1998, serving as its principal systems architect until Centillium Communications acquired the company. At Centillium, he managed development of customer premises equipment (CPE) products. Earlier in his career, he was a member of the research staff at Interval Research Corporation, a Paul Allen-funded think tank. At Interval, Ryan worked on digital media networking and next-generation consumer electronics, which led to the spin-off of Avio Digital as a separate company.

Ramachandran, who serves as director of microelectronics, was design manager at Avio Digital. He held the same position at Centillium after that company acquired Avio. At National Semiconductor, he managed the company's IP reuse methodology team and designed a co-processor for ARM-based systems. He began his career at LSI Logic.

Ron Abruzzese and Suresh Ram round out the management team as VP of sales and director of product marketing, respectively. Abruzzese most recently spent seven years at Winbond Electronics America, where he was VP of sales. He began as an IC design engineer at Texas Instruments, followed by several years as a digital systems design engineer at the Raytheon Company. He has also worked at TRW Electronics, Integrated Device Technology and Pericom Semiconductor.

During more than 10 years at National Semiconductor, Ram served as marketing manager for both the ADC and analog front-end product lines. He also held engineering and management responsibilities for quality assurance, failure analysis and reliability for a number of National's product lines.

Optichron has raised two rounds of funding. Its series A round came in two tranches; The $2 million tranche A1 came in Dec. 2002 from U.S. Venture Partners, which wanted to get the company off and running quickly. Tranche A2, for $7 million, closed with TL Ventures and VentureTechAlliance in June 2003. Battery Ventures led the March 2005 $17 million series B round, which included all of the A-round investors.

The company has not yet burned through its initial $9 million investment, and expects the latest series B round to last for two to two-and-a-half years. Optichron has 18 employees, which will likely grow to about 25 before the end of year.

The problem Optichron is solving, nonlinear distortion, is a form of signal-processing error that creates signals at frequencies not present in the input and occurs when the output signal does not have

a linear relation to the input signal. The new frequencies may be "harmonics," which exist at frequencies that are integer multiples of the tones present in the input signal. An everyday example of nonlinear distortion is a concave or convex mirror, in which the image is a nonlinear rendition of the reflected object.

In an electronics system, the output of signals traversing an amplifier, for example, or analog-to-digital converter (ADC) is contorted in a way very similar to a concave or convex mirror reflection. The resulting harmonics reduce bandwidth and performance.

However, nonlinear distortion is deterministic, so with the right math and technology it can be canceled. Optichron developed a new mathematical language that is the basis for its Turbolinear technology, which eliminates nonlinear distortion in many signal-processing applications.

Optichron's technology can address nonlinear distortion in a number of applications, but the company is focusing initially on ADCs. Optichron claims its Turbolinear family of nonlinear signal-processing modules removes more than 90% of the nonlinear distortion caused by not only the ADC, but the buffer amplifier as well.

The company's first two Turbolinear module products linearize ADCs from Analog Devices and Texas Instruments:

• OM1400A module: Incorporates Optichron's linearizer chip + 14-bit ADI AD6645 ADC + ADI 8351 amp.

• OM1400T module: Incorporates the linearizer + 14-bit Texas Instruments ADS5500 ADC + Watkins-Johnson Company AH22S amp.

Optichron's target applications are typically systems in which the imperative is performance, not cost. Designers of wireless receivers in base stations, for example, currently must do several stages of RF down conversion to get the signal between 0 MHz and 50 MHz so it can be quantized by an ADC; at higher frequencies, the nonlinearities are too high to quantize the signal. Optichron enables designers to eliminate the entire RF down-conversion stage, because the Turbolinear module can sample the signal at much higher frequencies and, according to the company, provide an output that is more linear than the use of a regular ADC in the 50-MHz range.

Another initial market focus is automated test equipment, where linearity is important just for its own sake. Optichron can enable these equipment vendors to build higher-performance systems with a 90-db linearity spec, for example, as opposed to a 60-db spec.

Other ADC module applications include:

- Multi-channel, multi-mode receivers;
- Base transceiver stations;
- Medical imaging;
- Communications instrumentation;
- Test and measurement;
- Scientific instruments; and
- Military radios.

The company divides its target markets into four segments: Small accounts, where 6,000 or 7,000 customers buy between 100 and 300 chips each per year from distributors; medium accounts, which are companies that buy in the range of 1000 chips per year; large accounts, represented by companies that purchase 25,000 to 50,000 chips annually; and OEMs that buy 150K to 500K per year.

While Optichron will never sell 20 million chips per year, the company's space is one where the prices and margins are high.

The company is currently working on two other data-converter ICs that are both at first silicon, as well as two chips not yet taped. Optichron will begin releasing more details this fall.

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Xceive

In the past, multi-standard TV tuners were not especially important to TV manufacturers, which typically employed different tuners for the world's different regions and standards. But these days, TV makers not only have different analog standards they have to address, they must also deal with the various digital standards adopted around the world. Xceive has developed a single-chip multi-standard TV tuner that will enable Asian TV products manufacturers for worldwide markets to standardize on one chip.

Founded in July 2001, Xceive is a 30-person company with a core team of engineers that have worked together more than 10 years. The company has raised $28 million dollars over three rounds of funding since inception, including a $13.5 million June 2005 series C round led by new investor Sequoia Capital. Alliance Ventures provided the $4 million series A round, and was joined by Ignite Group and BA Venture Partner Investors for the series $10.5 million series B round.

Xceive is headquartered in Santa Clara, Calif., and the company recently opened a design center in Switzerland and a five-person office in China. Xceive expects to turn the China office into a design center as well, although it will focus on applications and system development as opposed to IC development.

Xceive's two primary founders, both from Switzerland, are Pierre Favrat and Alain-Serge Porret. Favrat, who is president and CEO, was previously with the Advanced System Technologies group at STMicroelectronics, where he was analog/RF project leader for multimode cell phone circuits. Earlier, he worked for Motorola in its video design center in Geneva, Swityzerland.

Porret, the company's VP of engineering, was with a startup in San Jose, Calif., as principal engineer in charge of the system-level analysis of the company's VHF/UHF tuner chips. Prior to that he was a technical manager at Electronics Laboratory (LEG) at the Swiss Federal Institute of Technology and had co-founded a software development company.

Jordan Du Val joined Xceive in Jan. 2002 as VP of sales. He was previously president and CEO of SpotNet, a provider of two-screen interactive TV infrastructure services. He also held management positions at TeleCruz Technologies, S3, and was a founding member of the sales and marketing team at Genesis Microchip.

Alvin Wong, VP of marketing, joined Xceive in Dec. 2004. Wong was most recently at Infineon Technologies, where he was VP of marketing. Prior to that, he was with Philips Semiconductors in a number of key leadership roles.

Xceive developed a single-chip TV terrestrial/cable tuner that is not only capable of tuning to any standard on Earth, it is also very small, possesses high image quality and supports any form factor (LCD-TV, PCTV, cell phone TV, USBTV, plasma, etc.).

The company is in production with two products, and has engineering samples of a third. The company's first two products are the XC2028 and XC 3028. The XC2028 is a multi-standard analog tuner that supports all analog TV standard worldwide, while the XC3028 supports worldwide digital TV standards as well as analog TV standards.

The third product, the XC3510, is a highly integrated digital TV receiver for handheld devices. The chip is intended for DVBH, which is the digital mobile standard emerging in Europe.

Xceive's technology is centered on two developments. The first is its active filter and tracking filter technologies. A small microcontroller inside the chip constantly measures the signal quality throughout the tuner pipeline and, as the signal quality changes, adjusts the parameters of the filters for optimal performance. This is very different from a traditional can tuner architecture, in which the tuning parameters are set once and then shipped out in a product.

The other significant aspect of Xceive's chips is the very high level of integration. No external SAW filters or LNA is necessary. Instead of a bank of SAW filters, Xceive employs a bandpass filter, ADC and DSP to form the equivalent of a SAW filter. The company claims it can achieve an 80-db rejection, as opposed to the 50-db rejection achieved by the typical SAW filter. Xceive's chips therefore provide a very clean channel out to the demodulation back end.

The biggest market opportunity for Xceive is the TV market, a segment that is growing as people upgrade from analog to digital or hybrid (see Figure 4). In addition to TVs, applications adopting TV tuners include PVRs, DVD recorders, and laptop and desktop PCs. TV-enabled mobile phones will also likely emerge as a decent-size market over the next few years.

Xceive's sales are split about 50-50 between the XC2028 and XC3028, but it expects sales of the XC3028 to continue growing due to the growth of digital TV platforms.

Xceive works with a number of system chip providers on joint solutions, reference designs and manufacturing kits for various TV products. The company works with Conexant, for example, on joint designs and reference designs for PC-TV add-in cards, and with Pixelworks, Trident and Genesis on reference designs and manufacturing kits for LCD TVs. Other engineering partners include LSI Logic, Zoran, ATI and Micronas.

A number of customers are now in production ramp-up with Xceive's chips. These include Leadtek, which is developing an Xceive XC2028-based PC-TV tuner card, and AVerMedia, which is developing a mini-PCI TV card also based on the XC2028. Xceive is not yet disclosing other customers.

The main competitors in the silicon TV tuner market are the incumbent IDMs, especially Philips. On a bill of materials (BOM) comparison between the Philips TDA8275 and the XC2028, Xceive looks pretty good. The Philips TDA8275, for example, is a two-chip set plus an HPF and switch, and requires a much larger board area. According to Xceive, a PCI tuner card based on the TDA8275 has a BOM of $2.05, while a card based on its XC2028 has a BOM of $0.30.

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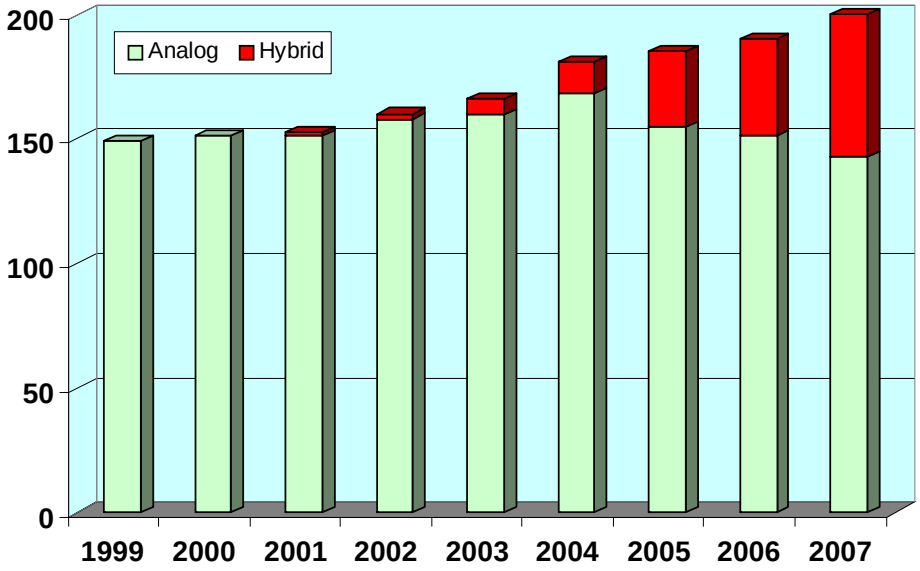
Figure 4 -- Global TV market (millions of units)



Source: Stanford Research and Allied Business Intelligence

JAM Technologies

Although amplifiers built on conventional analog technology are quite inefficient and have high heat dissipation, they still comprise about 95% of all amplifiers on the market. Switching amplifiers, or Class D amps, on the other hand, are very efficient and have low heat dissipation, but they are difficult to implement and the audio quality is often not very good. JAM Technologies has developed what it maintains is the only new approach to audio amplification in decades. The technology matches the sound quality of analog amps and the size and low heat generation of Class D amplifiers, and is sufficiently inexpensive to go into mass-market applications.

In business since 1999, JAM pursued a licensing and IP strategy for the first four years. In the fall of 2003, the company brought in about $3 million in angel funding and started down the path to a fabless model. JAM is currently in the middle of raising its series A venture funding, which will likely be in the $7 million range.

Larry Kirn and Jim Shanahan founded JAM. Kirn, who serves as president and CTO, invented and patented JAM's core technology for digital audio amplifier semiconductors as well as several key related technologies (18 issued and an additional 22 pending). Not surprisingly, he is an accomplished musician and expert in psychoacoustics. Previously, Kirn was an electrical engineering contractor to Chrysler, Ford and GM, and was responsible for design and development of electronic controller architectures and real-time operating systems for Chrysler concept vehicles. At Coy Laboratory Products, he was chief engineer of a medical equipment manufacturing firm, responsible for R & D as well as production.

Shanahan, the company's VP of corporate marketing, developed JAM Technologies from inception, executing all operating roles in the company outside of technology development. He has 15+ years in sales, marketing and business development, including the development of complex competitive proposals and market analysis.

Jean Hammond, a successful serial entrepreneur who participated in JAM's seed funding, is currently serving as interim CEO while the company conducts a CEO search. Hammond founded Quarry Technologies in 1998 together with a core team from the BBN Technologies/ GTE Internetworking SuperRouter project and served as president and CEO as well as chief strategy officer. In 1994, she co-founded AXON Networks, a developer of network management applications. Following 3Com's $65 million acquisition of AXON, Hammond was responsible for 3Com's WAN strategy, led the first venture investment by 3Com and the 3Com/ Newbridge/ Siemens deal. She has also held product-marketing positions at Index Technology, Spider Systems, and Racal-Redac.

JAM expects to bring in the new CEO and close its series A funding at the same time. The company is currently operating with quite a few contractors, so its true headcount is a little fuzzy. However, after the funding comes through, JAM expects to be in the 20-person range.

While the audio in consumer electronics is primarily digital, typical audio amplifiers continue to take an analog input and employ complex and/or expensive digital-to-analog converters (DACs). Direct digital-input amplifiers, therefore, are starting to emerge. However, the sigma-delta conversion technologies on which they are typically based are complex, require feedback loops and extensive signal processing, and result in higher silicon cost.

JAM calls its digital audio amplification E-Bridge, which the company markets under the trademark True Fidelity. E-Bridge refers to the switching amplifier output stage configuration, which bears a physical resemblance to the letter "E" (conventional switching amplifier output stages resemble the letter "H"). E-Bridge-based True Fidelity amplifiers, according to JAM, significantly outperform all competing Class D amp technologies as well as analog amplifiers.

All switch-mode amplifiers use output power devices as switches, achieving power amplification by converting the input signal to a sequence of pulses whose averaged value is directly proportional to the amplitude of the signal at that time. The output tends to create a lot of errors, nonlinearities and distortion, and many companies in this space focus on how to correct for the output stage.

JAM recognized that, no matter what measures are taken upstream, the maximum resolution in a switching amplifier system is limited to the minimum controllable time period of the output device. JAM maintains that unless GHz processing is used, the best resolution at the output stage for a 16-bit input is about 12 to 13 bits (If over-sampling is taken into account, the numbers are even worse). See Figure 5.

JAM determined that the best solution was to work within the limitations of a low-cost standard output stage. Much of the company's IP is based on taking the high-resolution incoming data stream and splitting it into one high-voltage low-resolution data stream and one low-voltage high-resolution

Figure 5 — Resolution required to play all 16 bits of a typical CD.

Sample period: 44,100
Data: 16 bits, or 2^{16}
or 65,536 bytes

16 bits of data in a 44,100 sample period equates to a resolution of 2^{16} x 44,100 or one part in 2,890,137,600

For a Class D amplifier to match that resolution, it must have switching speeds of 1/2,890,137,600, or 346 picoseconds (10^{-12})

data stream of equal portions (8 bits and 8 bits, for example in a 16-bit data stream). The company amplifies the data streams separately and then sums them across the load. Splitting the incoming digital data stream into two lower-resolution streams and summing them at the load enables E-Bridge to achieve high quality with vastly simplified logic.

In addition to sound quality, JAM claims it delivers a 30% cost advantage in the audio sub-system BOM, as compared to current solutions, because its simpler design requires fewer external components. E-Bridge eliminates the need for DACs, voltage regulators, PLLs, snubber circuits, the need for discrete volume control, and separate over/under voltage and current protection circuitry.

A number of applications are already using Class D amps. JAM believes its technology is initially most attractive to makers of flat panel LCD and plasma TVs, which do not have the capacity to handle hot spots behind the screen. Other early adopters include makers of bookshelf stereos, DVD and audio/video receivers.

JAM will soon introduce its first products, the MOZART family of digital-input amplifiers. The MOZART products are comprised of a two-channel, 7-watts-per-channel chip targeted at LCD, projection and flat-panel TV applications; and a two-channel, 20-watt-per-channel IC with the same features plus minimal heat sinking.

The company's second product, which samples in Q3 2005, is targeted at HTiB, AV, DVD and radio applications. The two-channel, 20-watt-per-channel chip has the same features as the first product, plus tone control and AM avoidance.

JAM sees other opportunities in games, playback stereo audio sources (FM radio, MP3, mobile TV, video clips), ringers, and multipoint video conferencing in which different call-parties are associated to different speakers.

The company also expects to work on integration plays with other companies, such as integrating its chip with other in-path chips, as well as finding opportunities in the cell phone and power management markets.

Out of the $80 million in Class D amps shipped in 2004, TI is the market leader with somewhere in the $30 million range of sales. Both Tripath and Apogee have each had yearly revenues as high as $15 million or so, although they are both currently south of that. National Semiconductor has a cell phone division for all types of amps, including Class D devices. Philips, the late entrant in this market, has nonetheless made big inroads.

Fortunately for JAM, consumer electronics manufacturers have a strong desire for efficient and cost-effective amplifiers, and they are generally eager to speak with any company claiming to have the next great Class D amplifier.

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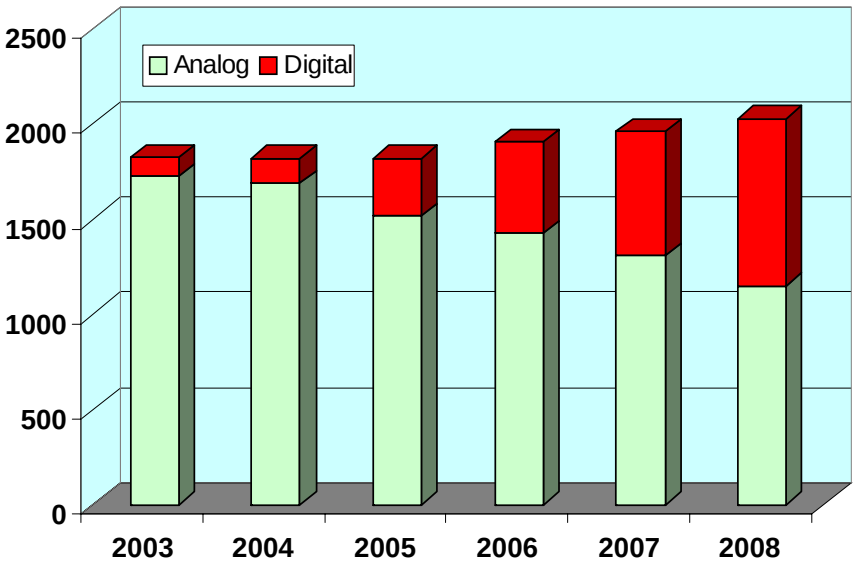
Figure 6 -- Audio amplifiers market ($ millions).



Source: Forward Concepts

EdXact

As the semiconductor industry moves to nanometer designs, the resulting explosion in data is overwhelming timing and simulation tools. France-based EdXact (which stands for Electronic Design: eXtraction, Analysis and Control Tools) is developing EDA tools that dramatically reduce the size of netlists, and consequently the simulation time, of complex digital and analog sub-100-nm ICs. The company claims that its first commercial set of tools, called JIVARO, can reduce netlist size by up to 99% and accelerate simulation by 10x to 100x, and more.

Three EDA veterans, Mathias Silvant, Stéphane Guédon and Frédéric Giroud, founded EdXact in April 2004. The founders came from Cadence Design Systems and, before that, Snaketech and Simplex. The entire 10-person team has worked together for the last seven years.

Silvant, who serves as EdXact's president, worked from 1994 to 1999 in industrial R&D projects with several companies, including Infineon Technologies, Philips Semiconductors and ZMD. He joined Snaketech, a company focusing on substrate parasitic extraction, in 1999, holding positions in customer support, R&D and management. Simplex Solutions acquired Snaketech in 2000, and Cadence subsequently acquired Simplex in 2002.

Guedon is EdXact's director of R&D. From 1994 to 1998, Guedon worked as a software project manager for GETRIS in the image-processing domain. Following that, he worked for the European Research Center of Xerox, and then joined Snaketech in 2000 as software manager. Following the Simplex and Cadence acquisitions, he developed numerical calculus algorithms

for various products.

Giroud, director development and industrialization, joined Snaketech in 1999 to develop interconnect and substrate parasitic extractions tools for custom ICs.

Even armed with brilliant ideas, French startups must often obtain their seed funding from sources other than venture capital firms, which are reluctant to invest in early-stage companies. EdXact obtained its initial funds by winning a governmental competition for innovative companies sponsored by the Ministry for Education and Research in 2004. The approximately $350,000 enabled EdXact to perform R&D for the first year.

In May 2005, EdXact closed its first seed round of financing with I-Source Gestion and Emertec Gestion, which provided the company with approximately $2.5 million.

Jivaro, EdXact's netlist-reduction tool, is named after a South American tribe of head shrinkers.

Designers are integrating ever-increasing amounts of functionality into smaller and smaller devices. Parasitic effects that in the past were insignificant must now be taken into account when verifying before they emerge as a source of failure at fabrication. The objective of netlist reduction is to reduce the number of parasitic elements in a circuit while maintaining its logical and electrical behavior.

Current techniques for dealing with parasitic effects explode the data volume and make analysis impossible. By reducing netlist data volumes, EdXact's Jivaro tool enables designers to perform multiple simulations in situations where data volumes previously prevented any kind of simulation.

While extracted parasitics overload existing timing and circuit-simulation tools, Jivaro's netlist-reduction capabilities reduce the overload to an acceptable level. The most significant benefit is reduced simulation turn-around times, which enable designers to explore different layout combinations and increase their chances of getting a design right.

Jivaro enables netlist reduction for all types of parasitic netlist components:

- R, RC, RLC, RLCK;
- Coupled, decoupled;
- Inductance, Mutual Inductance; and
- Substrate.

The problem with current netlist-reduction techniques, which typically involve smart filtering methods inside extraction and simulation software, is that accuracy is lost. But for sub-100-nm designs, as well as RF designs even at larger geometries, users must take into account capacitive coupling and even inductive coupling. EdXact claims that JIVARO is the first standalone netlist-reduction tool capable of accurately handling coupled capacitors, inductors and mutual inductors.

Jivaro is complementary to existing EDA tools from major vendors, and plugs into existing flows via its transparent interfaces based on SPICE, DSPF and SPECTRE file formats.

EdXact introduced two versions of JIVARO at the DAC Conference in June: JIVARO-A for analog and RF circuits, and JIVARO-D for digital and mixed-signal circuits.

According to EdXact, several semiconductor partners have evaluated JIVARO tools. For an RF circuit (LNA), DC simulation time dropped from 33 min. to 6 sec., a 330x speedup; and S-parameter analysis time dropped from 1hr. 40 min. to 9 sec., a 666x speedup. For a mixed-signal circuit (1-GHz ADC), transient spice simulation time dropped from one day to five hours. A digital ring oscillator's transient simulation –which at first proved unable to reach convergence — achieved convergence and correct results with the same simulator after adding JIVARO into the flow.

EdXact employs a time-based license model, typically for one or two years. The company says its license fee is equivalently priced to an option tool for a simulator.

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Northern Lights Semiconductor

Northern Lights Semiconductor Corp. (NLSC) is a Minnesota-based company developing high-performance magneto-resistive random access memory (MRAM) ICs. NLSC's technology, which it actually calls "EMRAM" for electromagneto-resistive RAM, is a non-volatile RAM that combines the fast read and write performance of SRAM with the high data storage capability of DRAM.

EMRAM combines many of the best features of different memory types, and NLSC hopes it will eventually replace current memory technologies such as SRAM, DRAM, ROM, EEPROM, flash, NVRAM, and FeRAM. The technology is easily embedded, and has a very small silicon footprint compared to other embedded memory technologies. (See Table 3 on page 18.)

NLSC says that EMRAM is especially effective in applications in which more than one memory type is deployed (such as SRAM + flash, SRAM+EEPROM, etc.) as well as in SOCs with a moderate or high percentage of silicon real estate committed to embedded memory. EMRAM is also inherently radiation hardened.

NLSC's primary founder is James Lai, who serves as the company's CEO and president. Lai spent 25 years at Honeywell, where he was the principal investigator of the Honeywell MRAM team that created world's first MRAM IC in operation today.

Lai originally launched the company in 1999 under the name Union Semiconductor Technology Corp. The company raised approximately $30 million from un-named Taiwanese investors, and bought a small, 6,000-square-foot fab from Cray Supercomputers. Union reorganized in 2004, changing its name to NLSC. NLSC is headquartered in Plymouth, Minn., and its fab is about 100 miles away in Chippewa Falls, Minn.

The management team also includes CTO Hsing-Kuen Liou, a Lucent Technologies veteran with extensive experience in IC design and manufacturing.

John Wagner, director of manufacturing, was chief engineer/chief scientist responsible for thin-film

metallization at Cray Research.

CFO Cynthia Schelske garnered extensive experience in financial management and "Big Four" public accounting.

K.C. Fong, VP of sales and marketing, has a background in aerospace engineering, systems and components marketing, and general management.

NLS employs about 20 people. Many are from Honeywell, and the company also picked up a few Cray people when it bought Cray's fab.

NLSC has significant metallization process capabilities and advanced packaging expertise, both central to the fabrication of embedded and stand-alone EMRAM ICs. The company has developed a family of parallel and serial standalone EMRAM devices with storage densities ranging from 4 Kb to 1 Mb. NLSC also offers embedded EMRAM (eEMRAM) up to 1 Mb for ASIC applications and SOCs.

The memory elements in a CPU are typically laid out next to the logic section, necessarily using up additional silicon real estate. By contrast, EMRAM layers sit on top of the logic CPU and any other peripheral, like a crowded city building up and not out. According to NLSC, this is a very high-yield architecture, as the EMRAM layers involve only a back-end metallization process. In addition, multiple (up to three) EMRAM layers can be stacked on top of the chip, creating higher density without increasing the footprint.

Compared to battery-backed SRAM and other NVRAM (such as FeRAM, SRAM flash packages), EMRAM offers equivalent performance at a far lower cost. Typically, says NLSC, replacing NVRAM with EMRAM will save the user more than 60% in component costs.

For example, customers can use eEMRAM in a smartcard microcontroller to replace multiple memory types (RAM, ROM and EEPROM). Another application is embedding eEMRAM on an RFID IC, replacing discrete EEPROM components. This lowers the cost of the resulting RFID IC package by more than 30%, says NLSC.

NLSC's initial products, which will be launched this year, are embedded MRAM (eMRAM) with density of up to 8 Mb, and MRAM devices with densities from 4 Kb to 16 Mb, which are targeted at battery-backed SRAM, SRAM-EEPROM package, SRAM-NOR flash combo-memory and select EEPROM/flash applications.

NLSC currently has samples available of 1-Mb EMRAM, 64 Kb EMRAM, and RFID with eEMRAM. The company's higher-density products will be available soon.

Available Q4 2005:

- 4 Mb,
- 8 Mb,
- 16 Mb, and
- 32 Mb.

Available Q2 2006:

- 64 Mb,
- 128 Mb, and
- 256 Mb.

Manufacturing EMRAM is currently a two-fab procedure that requires a conventional CMOS front-end process and a special back-end EMRAM metallization process that occurs that the Chippewa Falls metallization plant. The company's front-end partners are Mosel Vitelic for first-generation 0.5-micron CMOS and TSMC for second-generation 0.18-micron CMOS products.

NLSC expects to operate its back-end fabrication plant at least through 2006. After the technology has gained greater acceptance in the market, NLSC plans to work with one or more foundry partners to establish a line at (or next to) the foundry. At that point, the company's business model will shift and licensing/royalty would take on a more prominent role.

NLSC licenses its fundamental MRAM technology from Honeywell, one of the leaders in the MRAM space. Others include Freescale (formerly Motorola), Altis (a joint venture between IBM and Infineon), and TSMC. The necessary long-term investment and commitment has caused a number of players to exit the MRAM space, the latest being Cypress Semiconductor, which divested itself of MRAM subsidiary Silicon Magnetics in spring 2005.

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Table 3 -- Standalone memory comparison

Attribute	EMRAM	DRAM	SRAM	FLASH	EEPRO	FeRAM
High Density	**Yes**	Yes	No	Yes	No	No
Low Power	**Yes**	No	Yes	Yes	Yes	Yes
Non-volatile	**Yes**	No	No	Yes	Yes	Yes
Random Access	**Yes**	Yes	Yes	No	No	Yes
Non-destructive	**Yes**	No	Yes	Yes	Yes	No
No Wearout	**Yes**	Yes	Yes	No	No	No
Fast READ	**Yes**	Yes	Yes	Yes	Yes	Yes
Fast WRITE	**Yes**	Yes	Yes	No	No	Yes
Low WRITE Power	**Yes**	Yes	Yes	No	No	Yes
Ease to Embed	**Yes**	No	No	No	No	No
READ cycle	**5-100ns**	~100ns	5-100ns	~150ns	~150ns	50-150ns
WRITE cycle	**5-100ns**	~100ns	5-100ns	>1us	>10ms	50-150ns
WRITE Voltage	**<5V**	<5V 1	<5V	12V	12V	<5V
Data Retention Without Power	**INFINITE**	0	0	>10Y	>10Y	>10Y
Endurance						
(Number of Writes)	**>1E15**	>1E15	>1E15	~1E6	~1E5	~1E10
Relative Cel Size	**1**	1	4-Mar	1	1-1.2	1

Agreements and Marketing Alliances

ASAT and LSI Logic Enter Into Flip-Chip Cross-License Agreement

Semiconductor package design, assembly and test services provider ASAT Holdings has entered into a multi-year cross-licensing agreement with LSI Logic, under which LSI Logic will provide ASAT with a license to use its Flip Chip semiconductor package assembly technology. In addition, LSI Logic will certify ASAT's assembly process using copper/low K technology.

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Maniam Algarathanam, LSI Logic VP of advanced package development and assembly; Tel: 408 954-3108; www.lsilogic.com.

Calypto, Mentor Integrate Tools

EDA startup Calypto Design Systems is collaborating with Mentor Graphics to integrate the Calypto SLEC sequential equivalence checker with Mentor Graphics' Catapult C Synthesis tool, providing IC designers with a joint, verifiable, automated flow from an algorithmic chip description to an RTL description. To support these activities, Calypto has become a member of the Mentor Graphics OpenDoor partnership program.

With this integration, Catapult C users can automatically generate RTL from a pure ANSI C/C++ description, then automatically create SystemC "wrappers" containing verification directives and an interface mapping directly into the SLEC environment. This allows users to quickly verify functional equivalence between the pure ANSI C/C++ and RTL descriptions and quickly verify additional design optimizations before handing off to final IC implementation.

Founded in 2002, Calypto is attempting to bridge the gap between electronic system level (ESL) design and IC implementation with technology that enables designers to functionally verify their RTL designs much more easily and efficiently. Calypto's sequential equivalency checker technology provides designers with a tool that can determine whether higher-level models are functionally equivalent to their RTL implementations.

(See our profile of Calypto in the March 2005 issue of *InsideChips.Ventures*.)

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Shawn McCloud, Mentor high-level synthesis product manager; Tel: 503 685-7000; www.mentor.com.

IBM, Chartered and Samsung to Develop 65-nm Design Kits

IBM, Chartered Semiconductor Manufacturing and Samsung Electronics are jointly developing design kits for the 65-nm base and low-power processes. Specifically, the three companies will offer 65-nm designers common design kits that consist of physical verification (design rule checking (DRC) and layout versus schematic (LVS) matching) and parasitic extraction (RCX) technology files. Additionally, the companies will also make available common SRAM kits for single- and dual-port memories, eFUSE kit and electrostatic discharge (ESD) kit.

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Kevin Meyer, Chartered VP of worldwide marketing; Tel: (65) 6362.2838; www.charteredsemi.com.
KP Suh, Samsung exec. VP of technology development; Tel: +82-2-751-2986; www.samsung.com.

Avery Design, ASIC Architect Team to Deliver PCI Express IP Solution

Avery Design Systems and ASIC Architect have launched a cooperative effort to deliver a comprehensive PCI Express design and verification IP solution. Under the terms of the agreement, ASIC Architect and Avery will jointly promote their comprehensive solution to end users. Additionally, ASIC Architect has licensed Avery's PCI-Xactor solution to use for internal development.

The PCI-Xactor for PCI Express verification solution consists of Bus Function Model (BFM), SuperMonitor, and test suites and verification frameworks for functional verification of PCI Express components. The PCI-Xactor allows design and verification engineers to quickly and extensively test the entire functionality of their PCI Express-compliant devices. Verification frameworks form complete testbench environments for endpoint, switch, and bridge designs.

ASIC Architect develops high-performance, feature-rich PCI Express and advanced switching soft IP cores and solutions for FPGA and ASIC. ASIC Architect offers a wide range of PCI Express cores: endpoint cores, rootcomplex cores, root/endpoint port dual cores, switch port cores, and solution cores.

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Chilai Huang, Avery Design president; Tel: 978 689-7286; www.avery-design.com.

TI, Ember Team to Offer Low-Power ZigBee Chipset

Texas Instruments and Ember have established a collaboration to unveil the world's lowest-power-consuming ZigBee networking and microcontroller (MCU) platform. ZigBee is a wireless, standards-based radio technology for remote monitoring, control and sensor network applications.

Ember has paired its EM2420 802.15.4/ZigBee-compliant semiconductor platform with TI's MSP430F161x series of ultra-low-power MCU for developers building low-power ZigBee applications. TI's MSP430 platform of MCUs will also support Ember's next-generation EM260 network processor, which the company recently introduced.

The new dual-chip network module provides a complete, integrated MSP430 MCU, a radio and the ZigBee software platform. To reduce the device's footprint and BOM, the MSP430F161x MCU series integrates all peripherals, including high-performance analog and up to 55 KB of flash memory, which reduces the need for EEPROM. The device also features on-chip, high-precision control peripherals, such as a 12-bit 200k samples per second (ksps) analog-to-digital converter (ADC) and a 12-bit digital-to-analog converter (DAC) with a settling time of 1 microsecond.

Spun out of MIT in 2001 and based in

Boston, Mass., Ember develops ZigBee-compliant wireless semiconductor solutions for applications that range from home automation to making buildings consume less energy.

(See our profile of Ember in the Dec. 2003 issue of *InsideChips.Ventures*.)

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Faraday, Innovasic Enter into Strategic Partnership

ASIC and IP provider Faraday Technology and Innovasic Semiconductor, a supplier of ICs to the industrial automation market, have entered into a multi-year strategic partnership agreement. The agreement provides Innovasic and its customers with 10+ years of preferential supply in its upcoming products. In exchange, Faraday receives expertise and technologies that are necessary for mission-critical applications in harsh environmental conditions. The exchange is designed to enable both companies to expand their addressable markets.

With the adoption of Ethernet and embedded processors, the industrial market seems destined to converge with the PC-peripheral market. However, issues such as soft error rate under high radiation environment, and extremely low defective parts per million (PPM) — to name just two — are requirements quite different from Faraday's existing target markets. Through this partnership, Faraday expects to be better suited to address these issues.

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Keith Prettyjohns, Innovasic CEO; Tel: 505 883-5263; www.innovasic.com.

Rambus Signs Technology License Agreement with IBM

IBM has signed a new license agreement with Rambus to allow it access to Rambus's XDR memory controller interface cell, dubbed XIO. This agreement enables IBM to provide an advanced, high-speed design for high-performance consumer applications using Rambus's 90-nm ASIC process.

The Rambus XIO cell is a high-performance, low-latency controller interface to XDR DRAM memory sub-systems. It is a versatile CMOS macro cell that can be seamlessly integrated into a wide variety of target processes. The general-purpose cell is independent of the logical memory controller design, enabling support for a wide variety of memory applications needing high bandwidth and low latency. The XIO provides a wide, on-chip, CMOS-level signaling interface to the memory controller logic and a narrow, high-speed Differential Rambus Signaling Level (DRSL) interface to the external XDR memory system.

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Laura Stark, Rambus VP of platform solutions; Tel: 650) 947-5000; www.rambus.com.

SMIC, Magma Form Design Service Partnership

Magma Design Automation and Semiconductor Manufacturing International Corporation (SMIC) have established a formal partnership between the two companies. SMIC's Design Service Division is adopting Magma's integrated RTL-to-GDSII design solution — including Blast Create, Blast Plan Pro, Blast Fusion and Blast Power — for its ASIC design projects, as well as the SiliconSmart products for characterization and model creation of libraries and macros. To ensure successful adoption, a Magma support team will be on site at SMIC.

Each component of Magma's integrated RTL-to-GDSII solution for nanometer designs is based on a unified data model and uses the same timing, power and signal-integrity analysis and optimization engines. As a result, the Magma system enables designers to address key nanometer design issues such as on-chip variation considerations, complex physical design rules and noise avoidance during implementation.

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Business Microscope, Cont.

Continued from page 2

Matrix Semiconductor's 3-D architecture involves depositing multiple layers of active memory elements on a standard silicon substrate (or silicon surface) so that active circuitry is no longer confined to the silicon base, but extends vertically as well. The company has a ROM-type technology for building single-use flash memories, which are ideal for applications such as game cards. However, Matrix does not go beyond flash, and is unable to integrate analog and digital or multiple chips of different design types.

(See our profile of Matrix in the Jan. 2002 issue of *InsideChips.Ventures*.)

A spin-off of Japan's Tohoku University, ZyCube is developing a novel wafer-stacking technology in which different LSI wafers, which are independently fabricated, are stacked in three layers. The company has produced working prototypes of three-layer stacked image sensors, three-layer stacked memory chips, and three-layer stacked MPUs. The process relies on wafer alignment, wafer thinning, buried interconnections, micro-bumping and using an adhesive layer.

Vertical Circuits formed when TRW Components International merged with 3-D memory developer Cubic Memory in 1999. One of the company's specialties is manufacturing small-footprint, low-profile, stacked-die semiconductor packages for high-density, high-performance applications.

We believe Contour Semiconductor, still in stealth mode, is developing a 3-D architecture design and manufacturing process to serve the flash memory market.

3-D technology will reach the mainstream when design software and EDA tools become ubiquitous to designers, thermal management solutions become available, products demonstrate improved performance, yields prove to be acceptable, and manufacturing costs can match current 2-D solutions.

ASICs, IP and Design Services

FS2 Introduces Trace Tools For Sonics SiliconBackplane

First Silicon Solutions (FS2) has released the FS2 SB Navigator, a comprehensive trace and debug solution supporting Sonics SiliconBackplane SMART Interconnects. SB Navigator is a component of the Bus Navigator suite of FS2 products for system-level debug of complex embedded systems.

SB Navigator provides SOC developers with bus-level visibility to simplify and facilitate analysis of core-level intercommunications when developing complex SOCs. SB Navigator consists of an on-chip instrumentation block that connects through the SiliconBackplane snoop port to provide in-silicon-based triggering and trace, along with support for JTAG probe control and display system analysis software intercommunications. SB Navigator can be used standalone, or as part of FS2's Multi-core Embedded Debug on-chip instrumentation reference design for embedded silicon analysis, which includes multi-core system HyperDebug blocks, processor-specific in-system analyzer blocks, and other bus- and logic-specific instrumentation options.

Sonics is the developer of the SMART (Sonics Methodology and Architecture for Rapid Time to Market) Interconnect hardware solution. Sonics technology is essentially an on-chip communications system, a network comprised of interconnections between "agents" that communicate with each other and to an IP core.

(See our profile of FS2 in the Nov. 2004 issue of *InsideChips.Ventures*, and our profile of Sonics in the May 2003 issue).

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Bluespec Targets Low-Power ESL Synthesis

Bluespec, a developer of ESL synthesis for control logic and complex datapaths in chip design, has added low-power ESL synthesis with integrated clock and power management and formal clock verification capabilities to its ESL synthesis EDA toolset. Bluespec provides ASIC and FPGA engineers with the capability to validate proper multiple clock domain implementations during the synthesis process rather than delaying the discovery of synchronization issues in working silicon when they are hard and expensive to correct.

As SOCs continue to become larger and faster, gated clocks and multiple clock domains are increasingly used to manage power; support multiple, varied communication interfaces; and to re-use older IP that can demand different clock requirements. Synchronization issues are sometimes not discovered until the chip is manufactured into silicon. In addition, implementing and managing control logic around clock gating for power management is burdensome and contributes to design errors.

Bluespec has added integrated clock management and formal clock connectivity verification to enhance its multiple clock domain (MCD) support. Bluespec's toolset automates gated-clock implementations for power management by automatically identifying and managing interface communications between active and inactive clock domains. By incorporating clocking into its semantic model, Bluespec's toolset simplifies complex clock topology implementations and ensures that mis-connections are caught at the time of synthesis.

(See our profile of Bluespec in the March 2004 issue of *InsideChips.Ventures*.)

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Bits and Bytes, Cont.

Continued from page 3

ongoing informal inquiry into Lattice's prior restatement of financial results.

Lattice's special litigation committee, which was established for the purpose of conducting a review and investigation of the claims contained in two previously announced shareholder derivative complaints, brought these matters to the attention of the audit committee.

The suspensions came amid allegations of excessive bonuses for management and extravagant spending. The latest shareholder suits revealed that a company event in Hawaii included a private performance by singer Paul Anka – who, according to *The New York Times*, receives up to $350,000 for these kinds of events.

PMC-Sierra Eliminates 63 More Jobs

As part of an ongoing effort to improve its operating efficiency, PMC-Sierra is eliminating approximately 63 positions, primarily related to R&D, at a restructuring cost of approximately $5.9 million. The cuts are in addition to the 26 positions the company said it was eliminating in April at a restructuring cost of approximately $1.5 million. PMCS therefore expects to eliminate in aggregate approximately 89 positions — a workforce reduction of approximately 10% — at a total cost of approximately $7.4 million in Q2 2005. PMCS estimates the restructuring will reduce its operating expenses by approximately $10 million to $12 million per year.

PMCS currently has 902 full-time employees in its worldwide operations. The restructuring primarily relates to PMC's design and operations center in Santa Clara, Calif.

The addition of the 63 job cuts comes despite PMCS's expectation that its Q2 revenues will be at or near the high end of the revenue range provided in April. At that time, the company provided a revenue outlook of $70 million to $72 million for Q2, or 6% to 9% sequential growth. In addition, by the end of Q2, the company expects its book-to-bill ratio to exceed 1.1, as current quarter bookings are already greater than the company's Q2 revenue outlook.

The Fast Track ... People & Organizations

Sipex Appoints New CEO

Ralph Schmitt has joined Sipex as the company's new CEO. Schmitt, who will also be elected to the board of directors, most recently served as the executive VP of sales, marketing and business development at Cypress Semiconductor, where he was responsible for the transformation of the organization and strategy from a product-based to a market-based approach. He has also served on the boards of Cypress subsidiaries Silicon Light Machines and Cypress Microsystems, and also on the boards of privately held companies such as Azanda Networks and Stargen.

Schmitt started his career as a computer and communications system hardware designer and, in the mid-1990s, founded and ran his own manufacturers' representative firm.

Forte Expands Management and Sales Teams

Forte Design Systems has appointed two key executives, and opened its European headquarters in Grenoble, France.

Industry veteran Tom Katsioulas has joined Forte as Sr. VP of strategy and business development, and Brett Cline, formerly VP of marketing, has been promoted to VP of customer operations & services and corporate communications.

Prior to joining Forte, Katsioulas was a management consultant for EDA startups following his tenure as the founder and CEO of AmmoCore Technology. He has also held senior marketing positions at Cadence Design Systems and management and engineering positions at Tangent Systems and Digital Equipment Corp.

Cline's role has been expanded to include customer operations and support, in addition to corporate communications.

Francois Constant and Vincent Thibault will lead Forte's European headquarters in Grenoble.

Constant, head of European sales, previously held management positions at Summit Design and Synopsys. He was also co-founder and CEO of Arexsys.

Thibault joins Forte as European applications manager, and has held a wide variety of technical and management positions at Synopsys and Sagem Group.

Solarflare Communications Names VP of Marketing

Solarflare Communications has appointed Cyrus Namazi, formerly senior director of marketing and application engineering for Infineon Technologies Wireline Communications Group, as VP of marketing. Before joining Infineon, Namazi was employed at Broadcom, where he led Broadcom's foray into the ADSL market and spearheaded its market entry and strategic direction in the DSL market. Prior to Broadcom, he held various positions at AMD, where he was last responsible for strategic direction of communication and networking platforms. In spring 1998, he led the creation and launch of the Home Phoneline Networking Alliance (HomePNA) and served as its president and chairperson for more than two years. Prior to AMD, he worked at IBM/Lexmark in a variety of engineering and business positions.

Solarflare develops high-performance semiconductor solutions that enable existing networks to migrate to next-generation speeds without replacing the physical infrastructure.

(See our profile of Solarflare in the July 2004 issue of *InsideChips.Ventures*.)

Xilinx Appoints New CFO

Xilinx has appointed Jon Olson to the position of VP finance and CFO. Olson, currently VP of finance and enterprise services at Intel, will have the responsibility for finance, tax, treasury and investor relations at Xilinx.

Since joining Intel in 1979, Olson has held various senior financial positions, including VP of finance and enterprise services, director of finance, technology and manufacturing group controller, and semiconductor products group controller, as well as system manufacturing group controller. Prior to Intel, he worked for four years at General Signal.

Olson succeeds Kris Chellam, who will remain with the company in the role of senior VP, corporate and enterprise services. Chellam will continue to oversee information technology, internal audit, business and strategy development, real estate and the Asia/Pacific headquarters located in Singapore.

Intersil Promotes CTO to Exec. VP of WW Operations and Technology

Intersil has promoted Rajeeva Lahri to exec. VP of the Worldwide Operations and Technology Group. In addition, Lahri will continue to serve as the company's CTO. The Worldwide Operations and Technology Group includes information systems, worldwide procurement, packaging, process technology, operations planning, fab operations, test and assembly, and foundry operations.

Lahri has more than 23 years of experience in a variety of technology and operations roles. He joined Elantec in May 2001 as Sr. VP of technology and operations. In May 2002, after Intersil's acquisition of Elantec, he became CTO of Intersil. In Aug. 2003, Lahri took on overall responsibility for the company's global operations and technology organizations.

Earlier, Lahri held positions as Sr. VP and COO at Tessera Technologies, Sr. VP and deputy CTO at Philips Semiconductor, and Sr. VP of R&D and customer engineering at VLSI Technology.

Silicon Dimensions Names VP of Sales

Silicon Dimensions has appointed Craig Robbins VP of sales. Robbins previously served as VP of sales of Hier Design, a developer of next-generation hierarchical floorplanning and analysis software for FPGA design (acquired last year by Xilinx). Prior to Hier, he was the VP of sales of Silicon Perspective, and held executive management sales positions at Cadence Design Systems, Redwood Design Automation and Gateway Design Automation.

Founded in 2002, Silicon Dimensions launched an EDA tool suite intended to bridge the gap between logic design and physical design. The goal is to enable logic designers to pass to the physical design team a netlist that has an 80% to 85% potential for

closure on the first pass.

(See our profile of Silicon Dimensions in the July 2004 issue of *InsideChips.Ventures*.)

Tensilica Hires Sr. VP of Worldwide Sales

Antonio Viana has joined Tensilica as senior VP of worldwide sales. Viana worked for ARM since 1998 and held a number of positions during his tenure there, including business unit manager of development systems, director of the ARM foundry program, regional sales director and, for the past three years, VP of North American sales. Prior to ARM, he was director of sales for Encore Industries and worked for SGI and Hughes Aircraft.

SigmaTel Opens New Office in China

SigmaTel has opened a new office in Shenzhen, China. The Shenzhen office, which represents the third office opened by SigmaTel in Asia in six months, will provide direct, local support to its electronics-manufacturing customers in China.

The Shenzhen office has 16,964 square feet, three times larger than its existing Hong Kong Engineering Design Centre. Initially, SigmaTel will staff its Shenzhen office with up to 40 personnel, half of which will be engineers that will focus on applications support and development. Eventually, the facility will house more than 80 employees.

Aarohi Adds Senior VP of Software and Systems Engineering

Bill Huber has joined Aarohi Communications as senior VP of software and systems engineering. Prior to joining Aarohi, Huber served as CTO and VP of engineering at StoneFly Networks, a provider of cost-effective data protection and management solutions based on IP SANs. Previously, he was VP of software engineering at Nishan Systems (acquired by McData in 2003). Earlier, Huber co-founded test equipment company SIGnology (acquired by Tektronix), where he served as CEO.

Founded in 2001, Aarohi provides intelligent storage processors and intelligent storage adapters to storage system, network and server blade vendors.

(See our profile of Aarohi in the Sept. 2003 issue of *InsideChips.Ventures*.)

Intel Vet Takes on Strategic Planning Role at LSI Logic

LSI Logic has named Jeff Richardson executive VP of worldwide strategic planning. Previously, Richardson was VP of Intel's Digital Enterprise Group and GM of Intel's Server Platform Group. Earlier, he was VP and GM of Intel's Enterprise Solutions and Services Division, focusing on server and workstation building blocks for enterprise computing. Richardson became Intel's director of volume server development in the Enterprise Platforms and Services Division in 1997. He first joined Intel in 1992 as a senior design engineer for the company's Servers Business Unit. He has also served as a field applications engineer for Altera, senior microprocessor design engineer for Chips and Technologies, and as an ASIC design engineer for Amdahl.

Picolight Founder Joins Zarlink

Zarlink Semiconductor has appointed Stan Swirhun Sr. VP and GM of the company's optical electronics business. Swirhun is a founder and CEO of Picolight, a company specializing in vertical-cavity surface-emitting laser (VCSEL) -based optical components and transceivers. He led Colorado-based Picolight from 1997 to 2004 and, before that, was VP of engineering and then CTO at Vixel.

Zarlink also named Peter Burke as Sr. VP and GM of network communications, and Mike McGinn as VP of marketing communications and investor relations.

Netcell Adds Two to Executive Team

Storage processing specialist Netcell appointed Sanjay Adkar VP of engineering and Don Clegg VP of marketing.

Adkar joins Netcell from NeoMagic, where he was the corporate VP of engineering. Previously, he was at National Semiconductor as senior director of engineering in the Information Appliance group and at LSI Logic as director of ASIC design methodology.

Clegg most recently served as Tyan's VP of marketing and strategic sales. Prior to Tyan, Clegg held senior sales and marketing management positions at OPTi and Chips and Technologies, both core-logic silicon companies. He began his career as a design engineer for Northstar Computers and also held systems engineering positions at Wyse Technologies.

Netcell develops host adapter storage-acceleration devices for the ATA and SATA host bus adapter, consumer, server, workstation and embedded storage markets.

StarGen Launches Major Expansion into Asian Markets

StarGen is launching a major expansion of its sales organization into core Asian markets and has named Daniel Ip sales director. Ip, who will manage sales organizations in China, Korea, Taiwan and Southeast Asia, has more than 15 years of international semiconductor sales and business-development experience with companies such as PLX Technology and Adaptec. He will maintain an office in Hong Kong.

The company also appointed StarBridge as an authorized StarGen partner. StarBridge will maintain dedicated design and sales resources for StarGen's AXSys and StarFabric technologies.

In addition, Fuji Electronics has signed with StarGen to distribute the company's AXSys family of ASI products, and Trend-Tek China Company will be StarGen's distribution partner for China.

Conexant Hires New Senior VP of Worldwide Sales

Christian Scherp has joined Conexant Systems as senior VP of worldwide sales. Prior to joining Conexant, Scherp was VP and GM of Infineon Technologies North America's wireless/wireline communications group. Previously at Infineon, he served as VP of wireline communications products marketing, and VP and GM of the communications group's wide area networking business. Before the spin-off and creation of Infineon, Scherp held positions of increasing responsibility with Siemens in engineering, marketing, and business planning.

Companies Mentioned in This Issue