NEWS RELEASE

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STARC, Calypto and Virage Receive Editor's Choice Award from *Embedded Computing Design*

Flow to reduce dynamic and leakage power in SoCs for 40nm and below Highlighted in 'Deep Green' Section

SANTA CLARA, Calif. –– October 6, 2010 –– Calypto® Design Systems Inc. (www.calypto.com), the leader in sequential analysis technology, today announced *Embedded Computing Design's* Editor's Choice Award has been given to a low power design flow developed by Calypto, Virage Logic and the Semiconductor Technology Academic Research Center (STARC). Resulting from a multi-technology collaboration, the new seamless SoC design flow offers various functional modes to control multiple on-chip power domains for dramatic power savings. Initial results show up to 50 percent dynamic power reduction and up to 40 percent leakage power reduction in embedded SoC memories using Calypto's PowerPro MG tool and Virage Logic's SiWare memory compilers. The Editor's Choice Award recognizes technology that helps design "green" into today's new products.

"As performance rises and geometries shrink, designers are struggling to manage dynamic and leakage power in SOC designs," said Don Dingee, editorial director, *Embedded Computing Design* and OpenSystems Media. "On-chip memory accounts for a significant portion of the power budget. Through their collective focus on reducing memory power, Calypto, STARC and Virage enable designers to get more memory in embedded SoCs while still achieving 'green' designs."

About the Calypto/Virage/STARC Collaboration

Using Calypto's patented sequential analysis technology, PowerPro MG (for Memory Gating) constructs new memory gating logic that works in conjunction with the low-power memory modes in Virage Logic's SiWare memory compilers to produce the lowest power memory implementation possible. The SiWare memory compilers provide several different low-power modes – light sleep, deep sleep and power shut-off to allow designers to reduce leakage power when the memory is not being accessed. The compilers automatically generate PowerPro MG models enabling STARC to easily integrate PowerPro MG into their low power design flow.

"Receiving recognition for our continuous efforts to improve power efficiency is a testament to the importance of this issue for designers today," said Tom Sandoval, chief executive officer of Calypto. "Collaboration, such as this one between Calypto, Virage Logic, and STARC, is the most efficient way to make dramatic methodology improvements that enable our customers to deliver the most advanced, power-efficient designs ahead of their competition."

About OpenSystems Media

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About Calypto

Founded in 2002, Calypto® Design Systems, Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class power optimization and functional verification software, based on its patented sequential analysis technology. Calypto, whose customers include Fortune 500 companies worldwide**,** is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor program, Si2 and is an active participant in the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America. Corporate headquarters is located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. More information can be found at: www.calypto.com.

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