NEWS RELEASE

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STARC, Calypto and Virage Logic Break New Ground with Industry's Lowest Power Design Flow

Partnership enables complete, seamless flow to reduce dynamic and leakage power in SoCs for 40nm and below

SANTA CLARA, Calif. –– August 24, 2010 –– Calypto® Design Systems, Inc. (www.calypto.com), the leader in sequential analysis technology, today announced its collaboration with Virage Logic Corporation (NASDAQ: VIRL), and the Semiconductor Technology Academic Research Center (STARC) to dramatically reduce on-chip SoC power. Extending its ongoing, independent efforts with STARC and Virage Logic, the multi-technology collaboration resulted in the development of a seamless flow for designs with various functional modes that control multiple on-chip power domains to achieve dramatic power savings. Initial results show up to 50 percent dynamic power reduction and up to 40 percent leakage power reduction in embedded SoC memories using Calypto's PowerPro MG tool and Virage Logic's SiWare™ Memory compilers.

"Design teams are confronted with constant pressure to reduce SoC power. Without an automated flow to reduce memory power, designers are forced to engage in time-consuming analysis and error-prone manual modifications to the design," said Nobuyuki Nishiguchi, Vice President, General Manager, Development Department-1 at STARC. "Incorporating Calypto's PowerPro MG and Virage Logic's SiWare Memory IP into our low-power flow will enable designers to meet their design power goals in order to focus resources on bringing new levels of innovation to their products."

About Collaboration

Using Calypto's patented sequential analysis technology, PowerPro MG (for Memory Gating) constructs new memory gating logic that works in conjunction with the low-power memory modes in Virage Logic's SiWare Memory compilers to produce the lowest power memory implementation possible. The SiWare Memory compilers provide several different low power modes – light sleep, deep sleep and shut down to allow designers to reduce leakage power when the memory is not being accessed. The compilers automatically generate PowerPro MG models enabling STARC to easily integrate PowerPro MG into their low power design flow.

"STARC continues to contribute valuable, innovative design flows to the semiconductor industry," said Lisa Minwell, director of technical marketing for Virage Logic. "As the semiconductor industry's trusted IP partner and leading provider of embedded memories, we are pleased to collaborate with Calypto and STARC to enable mutual customers to deliver the most advanced, power-efficient designs possible."

"Reducing power in all of the key components of an SoC is critical to meeting today's competitive design goals," said Tom Sandoval, chief executive officer of Calypto. "Collaboration, such as this one between Calypto, Virage Logic, and STARC, is the most efficient way to make dramatic methodology improvements that enable our customers to deliver the most advanced, power-efficient designs ahead of their competition."

About Virage Logic

Virage Logic is a leading provider of both functional and physical semiconductor intellectual property (IP) for the design of complex integrated circuits. The company's highly differentiated product portfolio includes processor centric solutions, interface IP solutions, analog solutions, SoC infrastructure IP solutions, embedded SRAMs and NVMs, embedded memory test and repair, logic libraries, and memory development software. As the industry's trusted semiconductor IP partner, more than 400 foundry, IDM and fabless customers rely on

Virage Logic to achieve higher performance, lower power, higher density and optimal yield, as well as shorten time-to-market and time-to-volume. For further information, visit www.viragelogic.com.

About Calypto

Founded in 2002, Calypto® Design Systems, Inc. empowers designers to create high-quality, low-power electronic systems by providing best-in-class power optimization and functional verification software, based on its patented sequential analysis technology. Calypto, whose customers include Fortune 500 companies worldwide**,** is a member of the Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor program, Si2 and is an active participant in the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America. Corporate headquarters is located at: 2933 Bunker Hill Lane, Suite 202, Santa Clara, Calif. 95054. Telephone: (408) 850-2300. More information can be found at: www.calypto.com.

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