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Catapult C Synthesis Shines a Light on STMicroelectronics Imaging Challenges

The STMicroelectronics Imaging Division, within the company's Home Entertainment and Displays Group, creates high image quality products targeted at the consumer market. To achieve higher design productivity to compete more effectively in this demanding space, STMicroelectronics decided to investigate high-level synthesis solutions. Within just a few years, the division has gone from evaluating this methodology to relying on Calypto's high-level synthesis tool, Catapult®C Synthesis, to create some of its most critical designs. In fact, more that 70 million phones equipped with STMicroelectronics Imaging chips containing IP designed with Catapult C have been already sold.

STMicroelectronics Imaging Division develops a wide-range of sensors, camera modules, and image processors, building on 12 years of experience and expertise in the complete imaging chain (sensors, optics, processing). STMicroelectronics' image subsystems produce high image quality in compact form factors at a low cost and are mainly targeted at consumer products such as camera phones, PDAs, digital still cameras and optical mices. The division also creates sensors for dedicated optics in industrial and security applications along with imaging signal processors that implement advanced color processing and image enhancement algorithms.

STMicroelectronics was looking for a way to achieve higher design productivity when creating these high-quality, low-cost products. According to Arnaud Laflaquiere, Sensors Business Unit Manager in STMicroelectronics' Imaging Division, "The imaging market is a constant 'race to pixels' and sensor size, all of which is strongly dominated by time to market pressures."

"The image quality must constantly be improved through dedicated enhancement algorithms to differentiate image processor products," adds Massimo Mancuso, Image Processors Business Unit Manager within STMicroelectronics.

Power consumption must be kept to a minimum, since most of the imaging products end up in handheld devices that have strict power budgets to ensure competitive battery performance. However, sensor resolution directly impacts power:

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Massimo Mancuso
Image Processors
Business Unit Manager
STMicroelectronics

Alexandre Cellier, Massimo Mancuso, and Giuseppe Bonanno of STMicroelectronics.

the more pixels, the more power consumed. In addition, there is the constant tradeoff between using relatively power-hungry enhancement algorithms and optimizing for power.

Due to all these factors, multi-constraint optimizations are required in the imaging division's design environment. Flexibility, reactivity and the ability to quickly spin derivatives are absolutely essential to stay ahead in business.

Saving Time on First Designs

With all this in mind, Alexandre Cellier, Senior Design Engineer, and the ST Imaging design team decided a few years ago to investigate high-level synthesis. His team works in a C model-based flow where all the models for the designs are originally created in C/C++. The models are mostly bit accurate from the start. STMicroelectronics Imaging Division went through an extensive time-to-market improvement initiative, looking for ways to improve productivity. Their expectation was that high-level synthesis directed from the C models would enable the design team to achieve correct RTL quicker while improving the overall quality of the architectures. For example, it is faster to write a FIR filter in C without any timing or technology constraints than writing the same function in RTL. The RTL design requires the description of each of the different stages of pipeline needed to meet a given speed or technology target, making it a time-consuming task when designing at the RTL.

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Design Tools and Methodologies manager
STMicroelectronics

Cellier evaluated the Catapult C Synthesis solution from Calypto because it offered a mature and comprehensive environment for high-level synthesis. The assessment of Catapult C was to take place within the context of real-world design projects on three different design blocks.

The first IP block was a new algorithmic-based design that existed only as a higher-level description in C/C++. The second and third algorithm blocks were ones they had already created in RTL using the traditional hand coding approach. They decided to recreate these two from the original C specification in Catapult C. That would give them a direct comparison between the two methodologies with respect to design time and the quality of the RTL.

The results of all three evaluations surpassed the design team's expectations. The first IP was considered impossible to create in less than a year. Yet with Catapult C, the design team was able to deliver fully verified RTL in only 50 percent of the time. The second IP originally took six months to hand design, but it took only 10 weeks to create similar RTL results with Catapult C: a 60 percent time savings. The experience with the third IP was similar: it took five months to hand code the RTL compared to just three months with Catapult C, for a 40 percent reduction.

In all three test cases, the quality of the RTL—particularly with respect to area and timing—proved to meet or exceed the hand coded versions. These impressive results convinced the design team that high-level synthesis using Catapult C was a viable approach for the Imaging Division. In fact, they were so enthusiastic about Catapult C that by the end of that first year they had already taped-out their first IP block generated with Catapult C.

High Level Synthesis Expanding

Since that time, the STMicroelectronics Imaging Division has successfully taped out over 11 designs using high-level synthesis over the past four years.

The team has kept pace with a nearly 5X increase in design complexity in their imaging algorithmic IP during that time. They find it much easier to adapt and port their IP in C compared to RTL.

According to Cellier, "Our design team now routinely uses Catapult C to create complex, multi-block IP due to its maturity and its increasing capacity. Additionally, we face an on-going need to improve productivity to meet the increasing demands of the market." With more of the algorithmic design being automatically created by the high-level synthesis environment, less needs to be manually integrated in the later stages of the design.

Initially, the natural tendency was to design smaller, single blocks so the results could be easily understood as a check on whether Catapult C was creating acceptable, if not optimal results. Over time, the consistent quality achieved by Catapult C convinced them to move more of their algorithmic design to high-level synthesis. "As Catapult C earned our trust through predictable functional accuracy and high quality of result," says Cellier, "we gained the needed confidence to assign bigger designs to the tool, resulting in even larger productivity gains."

An Unexpected, Welcome Benefit

STMicroelectronics' imaging designers discovered that Catapult C considerably improved the reusability of their IP by moving the abstraction level from RTL to the C level.

Reuse at the RTL is far from straightforward and often a frustrating, time-consuming process. In many cases, RTL models are left poorly documented and the original IP authors are often busy with a new project or may not be with the company anymore. Despite strict coding guidelines, different IP usually looks different, based on the author's coding preferences. So it always takes time to get familiar with the coding and mindset of the author to understand the intent of the IP. Moreover, with complex algorithms, clever implementation tricks are often employed at the implementation level, making it even more difficult to understand the underlying algorithmic specification. All this makes it complicated to port an IP to a new, faster technology.

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In contrast, because the coding is done at the C level, with Catapult C the IP is easier to review and understand. The designers essentially focus on the functional intent, leaving most of the implementation details for the tool to automate, greatly facilitating later reuse and modifications. Verification is also greatly improved because the reuse of the IP is automated, eliminating errors that can creep in when hand coding RTL. Cellier offers a cautionary note, "While C/C++ is much more abstract than RTL, it is still easy to complicate it. Good guidelines and education are important for ease of readability and reusability, but once this learning investment is made, tremendous productivity gains can be obtained and sustained."

Moving Catapult C into Mainstream Design

Another welcomed advantage in adopting Catapult C was how easily it integrated into the team's design flow. As the Design Tools and Methodologies manager for the Imaging Division, Giuseppe Bonanno supports many EDA tools in the STMicroelectronics Imaging flows. He was pleased at how smoothly Catapult C was to adopt. "Catapult C proved to integrate quite seamlessly into our design flow. Initial glitches were resolved

expeditiously and Calypto's support was there every time we needed it."

Part of what smoothed the transition was the fact that the design team was already modeling their algorithmic IP in C/C++, so it was a natural progression to move to high-level synthesis. With Catapult C, the imaging designers can now create and refine the algorithms in C and then automatically create the RTL on the implementation side. Prior to Catapult C, making changes to the algorithms was a tedious and disconnected process. The modifications had to be hand coded in the RTL, creating a potential source of errors and requiring extensive, time-consuming debug cycles.

"With the Catapult C flow, RTL debug literally disappears. The C model is validated in its environment, and from there correct-by-construction RTL is created. This reduces the verification effort dramatically," Bonanno observes.

"In our product roadmaps, where the target frequencies are always increasing, we often have to rework existing IP to have it running at a higher frequency. Thanks to Catapult C we have drastically reduced the time required for retiming since all the modifications can be done at the C level," states Cellier.

An Ever-Expanding Horizon

Bonanno, Cellier, and the imaging design team are extremely satisfied with Catapult C for the creation of their algorithmic-based design IP. They plan to continue expanding its use in future designs. "We believe that Catapult C and high-level synthesis give us an important competitive edge," declares Mancuso. "It is one of many factors in helping us maintain our leadership in the highly competitive imaging market."

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